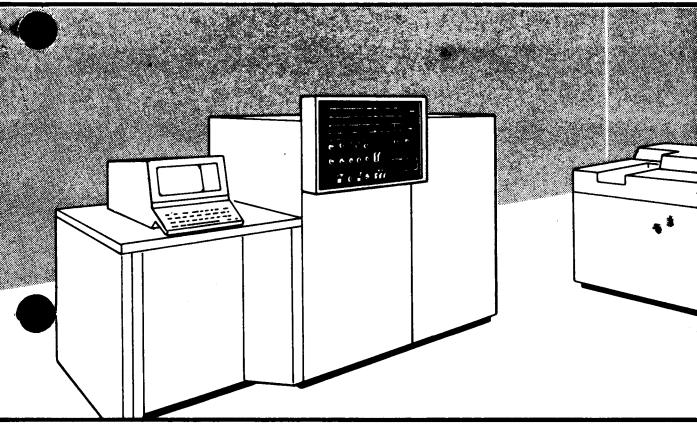
P. M. OMHOLT

MH2438

SPERRY UNIVAC PROCESSOR TYPE 3029-00 THRU -03

SERVICING REFERENCE DATA



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CUSTOMER ENGINEERING
JUNE, 1978

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HANDBOOK CHANGE BULLETIN

CUSTOMER ENGINEERING

EFFECTIVE DATE: SEPTEMBER 12, 1978

BOOK: MH2438 SPERRY UNIVAC
PROCESSOR TYPE 3029-00
THRU -03
SERVICING REFERENCE DATA

HCB-2

HANDBOOK APPLICATION

SPERRY UNIVAC 90/25, 90/30 and 90/30B	Miscellaneous

DESCRIPTION OF CHANGES

No data change locators (vertical bars in margin) are used in this revision to the book.

Processor Type 3029 Configurations
Is added to the book as an aid in correlating equipment to processor types.

Section Locator
Is updated to reflect section title changes and new sections added to the book.

Table of Contents
Is revised in accordance with changes made to the book.

Remaining Sections of the Book
The Scope of this book is expanded to include servicing reference data for the Processor Type 3029-02, -03. Also, information pertinent to the Processor Type 3029-00, -01 has been updated.

INSTRUCTIONS

All revised pages are labeled REVISION: HCB-2.

The entire book is reprinted to facilitate handling.
Replace the entire contents of MH2438 with the attached new pages.
Retain this HCB cover sheet behind the book's title page.

NOTE

Where information in this book is not applicable to the entire 3029 processor line, it is indicated by type number and system in parenthesis.

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PROCESSOR TYPE 3029
CONFIGURATIONS

	3029-00, -01 90/30 Below Ser. Nos. 746/J326	3029-00, -01 90/30	3029-02, -03 90/30	3029-02, -03 90/25	3029-02, -03 90/30B
7024 Memory	•				
MU40 Memory		•			
MU160 Memory			•	•	•
0717 Card Reader	•	•	•	•	•
0719 Card Reader				•	•
0605 Punch	•	•	•	•	•
0773 Printer	•	•	▼		
0778 Printer			•	•	•
U100 Console	•	•	•	•	•
8413 Diskette			•	•	•
8415 Disk				•	•
8416 Disk	•	•	▼		
8418 Disk	•	•	•	•	•
Selector Channels	•	•	•	•	•
Multiplexer Channel	•	•	•	•	•

• Available with system.
▼ Supplied by customer (previous purchase).

11866

SECTION LOCATOR

SECTION 1. PROCESSOR TYPE 3029-00 THRU -03 CENTRAL COMPLEX

SECTION 2. STORAGE

SECTION 3. IPC AND PERIPHERALS

SECTION 4. IDA AND PERIPHERALS

SECTION 5. SELECTOR AND MULTIPLEXER CHANNELS

SECTION 6. FOLDOUT ILLUSTRATIONS

Figure/Table	Title	Page
	SECTION 1. PROCESSOR TYPE 3029-00 THRU -03 CENTRAL COMPLEX	
1-1	Low Order Main Storage Assignments (3029-00,-01 90/30).	1-1
1-2	Low Order Main Storage Assignments (3029-02,-03 90/25, 90/30 and 90/30B).	1-4
1-3	IGR A Registers	1-7
1-4	IGR B Registers	1-8
1-1	Program Status Word (PSW) Format.	1-9
1-5	Program Status Word Description	1-9
1-2	Relocation and Protection	1-22
1-3	Key Address Format (Processor).	1-22
1-6	Key Address Format (Processor).	1-22
1-7	Interrupt Levels.	1-23
1-8	Interrupt Request Handling Priority Class	1-23
1-4	IOST Control Words.	1-24
1-9	IOST Control Word Bit Assignment.	1-25
1-5	Data Format	1-29
1-10	Decimal Data Code	1-29
1-11	OP Code, Mnemonic Code.	1-30
1-12	Symbols and Abbreviations	1-33
1-13	Instruction Repertoire.	1-34
1-6	Microword Format.	1-56
1-14	Microinstruction Format	1-57
1-15	BDW Microinstruction Format	1-58
1-16	Sense and Branch Group Ø.	1-60
1-17	Sense and Branch Group 1.	1-62
1-18	Sense and Branch Group 2.	1-64
1-19	Sense and Branch Group 3.	1-66
1-20	Sense and Branch Group 4.	1-68
1-21	Sense and Branch Group 5.	1-70
1-22	Sense and Branch Group 6.	1-72
1-23	Sense and Branch Group 7.	1-74
1-24	Sense and Branch Group 8.	1-76
1-25	Program Exception Equations	1-77
1-26	SAVE, IF, BLOCK Restrictions For Sense and Branch Conditions	1-78
1-27	Microinstruction Field Definitions.	1-79
1-28	Branch Address Formation-JC Field Addresses	1-99
1-29	Condition Code Equations.	1-100
1-30	Sense Information Listed By Register.	1-103
1-31	Program Exception Equations INT Statements.	1-108
1-32	COS Allocations	1-111
1-33	COS Chip Locations (1K-2K).	1-112
1-34	COS IC Locations (4K)	1-115
1-7	Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-00, -01,-02,-03 90/30).	6-1
1-8	Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-02, -03, 90/25 and 90/30B).	6-3
1-35	I/O Channel Number Assignments.	1-119

Figure/Table	Title	Page
	SECTION 2. STORAGE	
2-1	Memory Data Format.	2-1
2-2	7024 Memory Array Card (3029-00,-01 90/30 - Serial Numbers Below 746 or J326)	2-2
2-3	7024 Memory Address Format (3029-00,-01 90/30 - Serial Numbers Below 746 or J326) . .	2-3
2-1	7024 Memory Interface Signal Connections (3029-00,-01 90/30 Serial Numbers Below 746 or J326).	2-4
2-4	1103 Chip Description For 7024 Memory (3029-00, -01 90/30 - Serial Numbers Below 746 or J326)	2-7
2-5	MU40 Storage Unit (3029-00,-01 90/30)	2-8
2-2	MU40 Selection via ADRS 07-09 (3029-00,-01 90/30).	2-9
2-3	MU40 Card Column Selection Via ADRS 10-11 (3029-00,-01 90/30)	2-10
2-6	Memory Chip Layout on MU40 (3049-00,-01 90/30)	2-10
2-4	MU40 Data Bit Locations (3029-00,-01 90/30) . .	2-11
2-7	MU160 Fully Populated Storage Unit (1048K Bytes) (3029-02,-03 90/25, 90/30, and 90/30B)	2-12
2-8	MU160 Partially Populated Storage Unit (98.25K Bytes Maximum) (3029-02,-03 90/25, 90/30, and 90/30B)	2-13
2-9	MU160 Main Storage Addressing Scheme (3029-02, -03 90/25, 90/30, and 90/30B)	6-5
2-5	MU160 Address Decoding (3029-02,-03 90/25, 90/30B)	2-15
2-6	MU160 Jumper Installation (3029-02,-03 90/25, 90/30, and 90/30B).	2-16
2-7	MU160 Interface Pin Assignments (3029-02,-03 90/25, 90/30, and 90/30B)	2-17
2-8	I/O Channel Main-Storage Priority Order . . .	2-19
	SECTION 3. IPC AND PERIPHERALS	
3-1	IPC Buffer Control Word Format.	3-1
3-1	IPC Buffer Control Word	3-2
3-2	IPC IOSTIW Format	3-5
3-2	IPC IOST Interrupt Word Description	3-6
3-3	IPC SIO Condition Code.	3-8
3-4	Translate Mode Conversion	3-9
3-5	0717/0719 Card Reader Commands.	3-12
3-6	0717/0719 Card Reader Image Mode Conversion .	3-13
3-3	Summary of 0717/0719 Card Reader Status and Sense	3-14
3-7	0717/0719 Card Reader Status/Sense Bytes. . .	3-15
3-8	0605 Punch Commands	3-15
3-4	Summary of 0605 Punch Status and Sense. . . .	3-16
3-9	0605 Punch Status/Sense Bytes	3-17

Figure/Table	Title	Page
3-10	0773/0778 Printer Commands.	3-18
3-11	0773/0778 Printer Load Code Buffer Character Sequence.	3-19
3-5	0773/0778 Printer Buffer Locations.	3-20
3-6	Summary of 0773/0778 Printer Status and Sense	3-21
3-12	Printer Status/Sense Bytes.	3-22
3-13	U100 Console Command.	3-22
3-14	U100 Modifier Bit Description	3-23
3-7	Summary of U100 Console Status and Sense. . . .	3-24
3-15	U100 Console Sense and Status	3-25
3-16	U100 Console Status Bits.	3-25
3-8	U100 Console Cursor Addressing For Screen Display	6-6
3-17	EBCDIC to ASCII Translator.	3-27
3-18	ASCII to EBCDIC Translator.	3-28
3-19	U100 Console Data Byte Format	3-28
3-20	Character Set and Codes	3-29
3-21	U100 Console Codes.	3-30
3-22	8413 Diskette Subsystem Commands.	3-31
3-23	8413 FDC LED Indications For ILCS or IPL. . . .	3-32
3-24	8413 FDC Subsystem Functional Areas	3-32
3-9	8413 FDC Processor Control PC Board	3-33
3-10	8413 FDC PC Complement, Module 65	3-34
3-11	8413 Diskette FM Encoding	3-35
3-25	8413 Diskette Track Layout.	3-36
3-26	8413 Diskette Sector Layout (Ref. Figures 3-12 and 3-13)	3-36
3-27	Sector 5 Bad Track Data (Ref. Figure 3-12). . .	3-36
3-28	Sector 7 Volume Label Data (Ref. Figure 3-12)	3-37
3-29	Sectors 8-26 Track Data (Ref. Figure 3-13). . .	3-37
3-12	8413 Diskette Data Set Label Format Index Track Ø (Sector 01-07).	3-38
3-13	8413 Diskette Data Set Label Format Index Track Ø (Sectors 08-26)	3-39
3-30	8413 Diskette Sector Sequences.	3-40
3-14	Diskette FM Track Format.	6-7
3-31	8413 Diskette Status/Sense Error Conditions . .	3-42
3-32	8413 Diskette Status/Sense Byte Summary	3-44
3-33	8413 Diskette Error Table	3-45
3-34	8413 Diskette Recovery Procedure.	3-59

SECTION 4. IDA AND PERIPHERALS

4-1	IDA Commands and Codes.	4-1
4-1	IDA Buffer Control Words.	4-2
4-2	IDA Buffer Control Word	4-3
4-3	IDA Command Repertoire and Required BCW Field .	4-5
4-2	IDA IOST Interrupt Word	4-6
4-4	IDA IOST Interrupt Word	4-6
4-5	IDA Condition Codes	4-8
4-6	IDA Tag and File Bus.	4-8
4-3	Summary of Status Bits, Sense Bits, and Error Conditions (IDA).	6-8
4-7	IDA Sense Bytes	4-10

Figure/Table		Title	Page
	4-8	Summary of Sense Bits Possible For Each Command.	4-11
4-4		8416 and 8418 Disk Track Format (1).	4-12
4-5		8416 and 8418 Disk Track Format (2).	4-13
	4-9	Write Current Amplitude Per Cylinder Number. .	4-14
	4-10	Unsafe Display LED's	4-14
4-6		8416 Electronic Gate Unsafe LED Indicators . .	4-15

SECTION 5. SELECTOR AND MULTIPLEXER CHANNELS

5-1		CAW Format (Selector Channel).	5-1
	5-1	CAW Field Description (Selector Channel) . . .	5-1
5-2		CCW Format (Selector Channel).	5-1
	5-2	CCW Field Description (Selector Channel) . . .	5-2
5-3		Selector Channel IOSTIW Format	5-3
	5-3	Selector Channel IOSTIW Field Description. . .	5-3
	5-4	Channel Status Byte (Selector Channel)	5-4
	5-5	Command Codes (Selector Channel)	5-5
	5-6	Device Addresses (Selector Channel).	5-6
	5-7	SIO Condition Codes (Selector Channel)	5-6
	5-8	Setting of Error Conditions, CC = 01 (Selector Channel)	5-7
5-4		Buffer Control Word Format (Multiplexer Channel)	5-7
	5-9	Buffer Control Word Bit Assignments (Multiplexer Channel).	5-8
5-5		IOSTIW Format (Multiplexer Channel).	5-9
	5-10	Multiplexer Channel IOSTIW Description	5-10
	5-11	SIO Condition Code (Multiplexer Channel) . . .	5-11
	5-12	SIO Reject Conditions (Multiplexer Channel). .	5-12

SECTION 6. FOLDOUT ILLUSTRATIONS

1-7		Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-00,-01,-02,-03 90/30).	6-1
1-8		Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-02,-03 90/25 and 90/30B)	6-3
2-9		MU160 Main Storage Addressing Scheme (3029-02, -03 90/25, 90/30, and 90/30B).	6-5
3-8		U100 Console Cursor Addressing For Screen Display.	6-6
3-14		8413 Diskette FM Track Format.	6-7
4-3		Summary of Status Bits, Sense Bits, and Error Conditions (IDA)	6-8

SECTION 1

PROCESSOR
TYPE 3029-00 THRU -03
CENTRAL COMPLEX

REVISION: HCB-2

Table 1-1. Low Order Main Storage Assignments (3029-00, -01 90/30)

Byte Address	0 1 2 3	4 5 6 7	8 9 A B	C D E F
00X				
01X	IOSTCW0	IOSTCW1	IOSTCW2	(Reserved)
02X		IOST		IOST
03X		Mach. Check		Mach. Check
04X		Prog. Excep.		Prog. Excep.
05X	Old PSW	Supv. Call	New PSW	Supv. Call
06X		Interv.Timer		Interv.Timer
07X		(Reserved)		(Reserved)
08X		Monitor		Monitor
09X		(Reserved)		(Reserved)
0AX	CAW	MM LL RR 00	(Reserved)	
0BX	Rel. Reg. 0	Rel. Reg. 1	Rel. Reg. 2	Rel. Reg. 3
0CX	Rel. Reg. 4	Rel. Reg. 5	Rel. Reg. 6	Rel. Reg. 7
0DX	(Reserved)			
0EX	(IOST BCSW)			
0FX	Int. Disk BCW0	Int. Disk BCW1	Int. Disk BCW2	Int. Disk BCW3
10X	Console BCW0	Console BCW1	Console BCW2	Console BCW3
11X	Reader BCW0	Reader BCW1	Reader BCW2	Reader BCW3
12X	Printer BCW0	Printer BCW1	Printer BCW2	Printer BCW3
13X	Punch BCW0	Punch BCW1	Punch BCW2	Punch BCW3
14X	LA0(CA1)BCW0	LA0 BCW1	LA0 BCW2	LA0 BCW3
15X	LA6 BCW0	LA6 BCW1	LA6 BCW2	LA6 BCW3
16X	LA1 BCW0	LA1 BCW1	LA1 BCW2	LA1 BCW3
17X	LA7 BCW0	LA7 BCW1	LA7 BCW2	LA7 BCW3

Table 1-1. Low Order Main Storage Assignments (3029-00, -01 90/30) (cont)

Byte Address	0 1 2 3	4 5 6 7	8 9 A B	C D E F
18X	LA2 BCW0	LA2 BCW1	LA2 BCW2	LA2 BCW3
19X	LA8 BCW0	LA8 BCW1	LA8 BCW2	LA8 BCW3
1AX	LA3 BCW0	LA3 BCW1	LA3 BCW2	LA3 BCW3
1BX	LA9 BCW0	LA9 BCW1	LA9 BCW2	LA9 BCW3
1CX	LA4 BCW0	LA4 BCW1	LA4 BCW2	LA4 BCW3
1DX	LA10 BCW0	LA10 BCW1	LA10 BCW2	LA10 BCW3
1EX	LA5 BCW0	LA5 BCW1	LA5 BCW2	LA5 BCW3
1FX	LA11 BCW0	LA11 BCW1	LA11 BCW2	LA11 BCW3
20X	Mux.Subch, 0 BCW0	Mux.Subch. Subch.0 BCW1	Subch.0 BCW2	Subch.0 BCW3
21X	Subch.1 BCW0	Subch.1 BCW1	Subch.1 BCW2	Subch.1 BCW3
22X	Subch.2 BCW0	Subch.2 BCW1	Subch.2 BCW2	Subch.2 BCW3
23X	Subch.3 BCW0	Subch.3 BCW1	Subch.3 BCW2	Subch.3 BCW3
24X	Subch.4 BCW0	Subch.4 BCW1	Subch.4 BCW2	Subch.4 BCW3
25X	Subch.5 BCW0	Subch.5 BCW1	Subch.5 BCW2	Subch.5 BCW3
26X	Subch.6 BCW0	Subch.6 BCW1	Subch.6 BCW2	Subch.6 BCW3
27X	Subch.7 BCW0	Subch.7 BCW1	Subch.7 BCW2	Subch.7 BCW3
28X . . 2FX	(Not Used)			
30X . . 33X	(Reserved)			
34X	LA0(CA2) BCW0	LA0 BCW1	LA0 BCW2	LA0 BCW3
35X	LA6 BCW0	LA6 BCW1	LA6 BCW2	LA6 BCW3
36X	LA1 BCW0	LA1 BCW1	LA1 BCW2	LA1 BCW3
37X	LA7 BCW0	LA7 BCW1	LA7 BCW2	LA7 BCW3

Table 1-1. Low Order Main Storage Assignments (3029-00, -01 90/30) (cont)

Byte Address	0 1 2 3	4 5 6 7	8 9 A B	C D E F
38X	LA2 BCW0	LA2 BCW1	LA2 BCW2	LA2 BCW3
39X	LA8 BCW0	LA8 BCW1	LA8 BCW2	LA8 BCW3
3AX	LA3 BCW0	LA3 BCW1	LA3 BCW2	LA3 BCW3
3BX	LA9 BCW0	LA9 BCW1	LA9 BCW2	LA9 BCW3
3CX	LA4 BCW0	LA4 BCW1	LA4 BCW2	LA4 BCW3
3DX	LA10 BCW0	LA10 BCW1	LA10 BCW2	LA10 BCW3
3EX	LA5 BCW0	LA5 BCW1	LA5 BCW2	LA5 BCW3
3FX	LA11 BCW0	LA11 BCW1	LA11 BCW2	LA11 BCW3

Table 1-2. Low Order Main Storage Assignments
(3029-02, -03 90/25, 90/30 and 90/30B)

Byte Address (Hexa-Decimal)	0 1 2 3	4 5 6 7	8 9 A B	C D E F
00X				
01X	IOSTCW0	IOSTCW1	IOSTCW2	(Reserved)
02X	IOST	Old PSW	IOST	New PSW
03X	Mach.Check	Old PSW	Mach.Check	New PSW
04X	Prog.Excep.	Old PSW	Prog.Excep.	New PSW
05X	Supv. Call	Old PSW	Supv. Call	New PSW
06X	Interv.Timer	Old PSW	Interv.Timer	Old PSW
07X	(Reserved)		(Reserved)	
08X	Monitor	Old PSW	Monitor	Old PSW
09X	(Reserved)		(Reserved)	
0AX	CAW	MM LL RR 00	(Reserved)	
0BX	Rel.Reg.0	Rel.Reg.1	Rel.Reg.2	Rel.Reg.3
0CX	Rel.Reg.4	Rel.Reg.5	Rel.Reg.6	Rel.Reg.7
0DX	(Reserved)		(Reserved)	
0EX	IOST BCSW		IOST BCSW	
0FX	Int. Disk BCW0	Int. Disk BCW1	Int. Disk BCW2	Int. Disk BCW3
10X	Console BCW0	Console BCW1	Console BCW2	Console BCW3
11X	Reader BCW0	Reader BCW1	Reader BCW2	Reader BCW3
12X	Printer BCW0	Printer BCW1	Printer BCW2	Printer BCW3
13X	Punch BCW0	Punch BCW1	Punch BCW2	Punch BCW3
14X	LA0 BCW0	LA0 BCW1	LA0 BCW2	LA0 BCW3 } Single
15X	LA6 BCW0	LA6 BCW1	LA6 BCW2	LA6 BCW3 } CA or
16X	LA1 BCW0	LA1 BCW1	LA1 BCW2	LA1 BCW3 } Dual CA

Table 1-2. Low Order Main Storage Assignments (3029-02, -03 90/25, 90/30 and 90/30B)(cont)

Byte Address (Hexadecimal)	0 1 2 3	4 5 6 7	8 9 A B	C D E F	
17X	LA7 BCW0	LA7 BCW1	LA7 BCW2	LA7 BCW3	Single CA or Dual CA
18X	LA2 BCW0	LA2 BCW1	LA2 BCW2	LA2 BCW3	
19X	LA8 BCW0	LA8 BCW1	LA8 BCW2	LA8 BCW3	
1AX	LA3 BCW0	LA3 BCW1	LA3 BCW2	LA3 BCW3	
1BX	LA9 BCW0	LA9 BCW1	LA9 BCW2	LA9 BCW3	
1CX	LA4 BCW0	LA4 BCW1	LA4 BCW2	LA4 BCW3	
1DX	LA10 BCW0	LA10 BCW1	LA10 BCW2	LA10 BCW3	
1EX	LA5 BCW0	LA5 BCW1	LA5 BCW2	LA5 BCW3	
1FX	LA11 BCW0	LA11 BCW1	LA11 BCW2	LA11 BCW3	
20X	Mux. Subch.0 BCW0	Mux. Subch.0 BCW1	Mux. Subch.0 BCW2	Mux. Subch.0 BCW3	
21X	Subch.1 BCW0	Subch.1 BCW1	Subch.1 BCW2	Subch.1 BCW3	
22X	Subch.2 BCW0	Subch.2 BCW1	Subch.2 BCW2	Subch.2 BCW3	
23X	Subch.3 BCW0	Subch.3 BCW1	Subch.3 BCW2	Subch.3 BCW3	
24X	Subch.4 BCW0	Subch.4 BCW1	Subch.4 BCW2	Subch.4 BCW3	
25X	Subch.5 BCW0	Subch.5 BCW1	Subch.5 BCW2	Subch.5 BCW3	
26X	Subch.6 BCW0	Subch.6 BCW1	Subch.6 BCW2	Subch.6 BCW3	
27X	Subch.7 BCW0	Subch.7 BCW1	Subch.7 BCW2	Subch.7 BCW3	
28X	(UNUSED)				
29X					
2AX					
2BX					
2CX					
2DX					

Table 1-2. Low Order Main Storage Assignments
(3029-02, -03 90/25, 90/30 and 90/30B)(cont)

Byte Address (Hexadecimal)	0 1 2 3	4 5 6 7	8 9 A B	C D E F	
2EX 2FX	(UNUSED)				
30X	DR0 BCW0	DR0 BCW1	DR0 BCW2	DR0 BCW3	
31X	DR1 BCW0	DR1 BCW1	DR1 BCW2	DR1 BCW3	
32X	DR2 BCW0	DR2 BCW1	DR2 BCW2	DR2 BCW3	
33X	DR3 BCW0	DR3 BCW1	DR3 BCW2	DR3 BCW3	
34X	LA0 BCW0	LA0 BCW1	LA0 BCW2	LA0 BCW3	
35X	LA6 BCW0	LA6 BCW1	LA6 BCW2	LA6 BCW3	
36X	LA1 BCW0	LA1 BCW1	LA1 BCW2	LA1 BCW3	
37X	LA7 BCW0	LA7 BCW1	LA7 BCW2	LA7 BCW3	
38X	LA2 BCW0	LA2 BCW1	LA2 BCW2	LA2 BCW3	
39X	LA8 BCW0	LA8 BCW1	LA8 BCW2	LA8 BCW3	Dual CA
3AX	LA3 BCW0	LA3 BCW1	LA3 BCW2	LA3 BCW3	No. 2
3BX	LA9 BCW0	LA9 BCW1	LA9 BCW2	LA9 BCW3	
3CX	LA4 BCW0	LA4 BCW1	LA4 BCW2	LA4 BCW3	
3DX	LA10 BCW0	LA10 BCW1	LA10 BCW2	LA10 BCW3	
3EX	LA5 BCW0	LA5 BCW1	LA5 BCW2	LA5 BCW3	
3FX	LA11 BCW0	LA11 BCW1	LA11 BCW2	LA11 BCW3	

*NOTES:

1. MM = MACHINE MICROCODE ID FIELD.
2. LL = LOAD MICROCODE ID FIELD.
3. RR = REVISION LEVEL MICROCODE ID FIELD
4. 00 = ZERO FILLER.

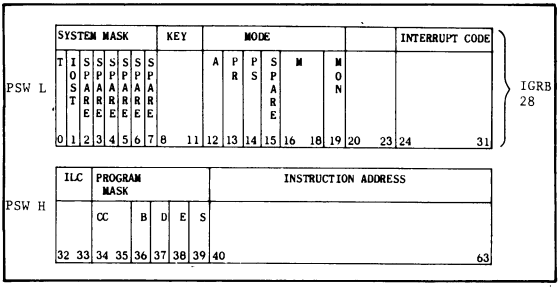

Figure 1-1. Program Status Word (PSW) Format

Table 1-5. Program Status Word Description

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
			NOTE System mask interrupts (bits 0-7) are active if set to 1.
M	Ø	T	Timer Level Interrupt Mask
A			Ø = Inhibit Interrupt 1 = Allow Interrupt
S	1	IOST	To mask Equipment Crack error and I/O Status Tabler Level (7) Interrupt Mask. Ø = Inhibit Interrupt 1 = Allow Interrupt
K	2		Not Used, Must = Ø
	3		
	4		
	5		
	6		
	7		
	8		Always = Ø
K	9		Storage Protection and Relocation Key.
E	10		Indicates the job presently active in the central processor. Assigns blocks of main storage in either 512/1024/2048
Y	11		byte blocks.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT	BIT POS.	NAME	FUNCTION
	12	A	0 = EBCDIC mode select 1 = ASCII mode select
	13	PR	0 = Supervisor General Register select
M			1 = Problem General Register select
O	14	PS	0 = Supervisor mode select
D			1 = Problem mode select
E	15		Unassigned, must = Ø
	16		M Field 000 = 90/30 Native mode
	17		M Field 001 = 9200/9300 Compatibility mode
	18		M Field 010 = 360/20 Compatibility mode
	19	MON	0 = Normal mode select 1 = Monitor mode select
U	20		Must = Ø
N			
A	21		
S			
S	22		
I			
G	23		
N			
E			
D			

Table 1-3. IGR A Registers

Reg. No. Hex.	Program Register Adr.	PR-Bit in PSW 13	Hardware Generated	Description
0	-	-	000000	Current Instruction Halfword
1	-	-	000001	1st Operand Address (Absolute)
2	-	-	000010	2nd Operand Address (Absolute)
3	-	-	000011	Working Register
4	-	-	000100	Working Register
5 ↓	-	-	000101 ↓	Working Register ↓
F	-	-	001111	Working Register

Table 1-4. IGR B Registers

Bank	Reg. No. Hex.	Program Register Adr.	PR-Bit In PSW 13	Hardware Generated	Description
	00	0000	0	000000	Supv. Gen. Reg.0
	01	0001	0	000001	Supv. Gen. Reg.1
1	02	0010	0	000010	Supv. Gen. Reg.2
	03	0011	0	000011	Supv. Gen. Reg.3
	↓				↓
	0F	1111	0	001111	Supv. Gen.Reg.15
	10	0000	1	010000	Prob. Gen. Reg.0
	11	0001	1	010001	Prob. Gen. Reg.1
2	12	0010	1	010010	Prob. Gen. Reg.2
	13	0011	1	010011	Prob. Gen. Reg.3
	↓				↓
	1F	1111	1	011111	Prob. Gen.Reg.15
	20	0000	-	100000	Float.Pt. Reg. 0
	22	0010	-	100010	Float.Pt. Reg. 2
3	24	0100	-	100100	Float.Pt. Reg. 4
	26	0110	-	100110	Float.Pt. Reg. 6
	28	-	-	101000	Current PSW Inst. Address
	29	-	-	101001	Current Relocation Reg.(OFFSET)
3	2A	-	-	101010	Working Reg. 2
	2B	-	-	101011	Working Reg. 3
	2C	-	-	101100	Working Reg. 4
	↓				↓
	2F	-	-	101111	Working Reg. 7

NOTE: 16 supervisor general registers (32 bits)
16 problem general registers (32 bits)
4 double-word floating-point registers (64 bits)
8 working registers, for microprogram use (32 bits)

Table 1-5. Program Status Word Description (continued)

PSW FORMAT	BIT POS.	NAME	FUNCTION
I N T E R R U P T C O D E	24 TO 31		Processor Machine Check Class (a) 11100101 - Address Exception or Protection Exception on a processor control hardware generated address. (b) 11100110 - A Control Storage Write Bus Check occurs during the execution of the LCS instruction. (c) 11100111 - A Storage Parity Check occurs on any processor reference except those which generate a non-recoverable error. (d) 11101000 - An Address Check occurs on any processor reference except those which generate a non-recoverable error. (e) 11101100 - A Program Exception interrupt request occurs and the Program Exception hardware mask (PX) is set. (f) 11101111 - The Processor Stall Timer expires during processor instruction execution or IIS execution.

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Table 1-5. Program Status Word Description (continued)

PSW FORMAT	BIT POS.	NAME	FUNCTION
			Lost Machine Check Class (a) 00000101 - Address Exception or Protection Exception while addressing IOSTCW. (b) 00001000 - Address Check or Data Parity Error while addressing IOSTCW. (c) 00001111 - Processor Stall Timer expired during IOST sequence. Equipment Check Class (a) 11100000 - Early Warning Temperature fault detected. PROGRAM EXCEPTION LEVEL NOTE The following table summarizes the results if an instruction (that examines both the System Mask and the Hardware Mask) generates an interrupt request.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION

Program Mask	Hardware Mask (PX)	Hardware Mask (MC)	Result
0	X	X	Instruction processing continues with no pending interrupt request, no Non-Recoverable Error, and no Program Exception interrupt.
1	X	set	Non-Recoveralbe Error
1	cleared	cleared	Program Exception IIS and set PX Hardware mask.
1	set	cleared	Machine Check IIS and set MC Hardware mask.

Note: X denotes bit ignored.

(a) 00000001 - Operation Exception

An illegal operation has been attempted or an operation using a non-installed processor feature has been attempted.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
			(b) 00000010 - Privileged Operation Exception A privileged operation has been attempted by a program operating in the Problem Mode (PS, bit 14 of the current PSW, set to one). (c) 00000011 - Execute Exception The subject instruction of an Execute instruction is an Execute instruction. (d) 00000100 - Protection Exception A storage protection violation occurs on a program generated address, when the Storage Protect Feature (F1622-00) is installed. (e) 00000101 - Addressing Exception A storage location outside the range of the installed storage is referenced by a program specified address. For the Load Control Storage instruction only, the referenced control storage location is non-existent.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
			Timer An Interval Timer is provided as an integral part of the 90/30 Processor. The Timer count, located in a 24-bit Interval Timer Register (ITR), will be decremented once every millisecond if it is turned ON via the STR instruction. The binary count contained in the ITR allows the interval between interrupts to range from one millisecond to 4.66 hours. An Interval Timer Interrupt Request will occur whenever the ITR count steps from 1 to 0. I/O Status Tabler An IOST Interrupt Request occurs when the IOST Interrupt Request Flip-Flop (IRF) is set and the System Mask bit (bit 1 is the PSW) is a one. If the mask bit is zero, the interrupt will remain pending until the mask bit is set to one. When allowed, the interrupt request will enter and IIS for the IOST level. Interrupts of this level may occur only after execution of the current processor instruction is completed. The ILC stored in the old PSW is zero, and the interrupt code in the IOST old PSW will be cleared to zeros. Monitor The level of interrupt is utilized by the Monitor Mode. The System Mask does not apply to this level. Zeros are inserted in the Interrupt Code associated with this level.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
			The MON bit, (bit 19 in current PSW), specifies the Monitor mode. The monitor interrupt indicates that a processor instruction has been completed and the next instruction may be premonitored. All instructions are completed in this level of interrupt and the ILC stored in the old PSW is zero.
I L C	32 and 33	ILC	The ILC reflects the number of halfwords to subtract from the current instruction being interrupted as follows:

ILC	PSW Bits 32	PSW Bits 33	Instruction Length	Instruction Format	Sub. From IGRB 28
0	0	0	Instr.Complete	-	0
1	0	1	One ½ word	RR	2
2	1	0	Two ½ words	RX, RS, SI	4
3	1	1	Three ½ words	SS	6

P R O G R A M M A S K	34 and 35	CC	Condition Code Indicates the result of the previous instruction executed. Possible codes for all instructions are listed in Instruction Groups/Condition Codes in the book.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
			(i) 00001001 - Fixed-Point Divide Exception The quotient of a fixed-point divide operation exceeds the capacity of the first operand (including division by zero) or the result of a Convert to Binary instruction exceeds 31 bits.
			(j) 00001010 - Decimal Overflow Exception The result of an Add Decimal, Subtract Decimal, or Zero and Add instruction exceeds the capacity of the first operand location. This interrupt is masked by D (bit 37 of the current PSW).
			(k) 00001011 - Decimal Divide Exception The quotient of a Divide Decimal instruction exceeds the capacity of the quotient part of the first operand field.
			(l) 00001100 - Exponent Overflow Exception The final characteristic resulting from a floating-point arithmetic operation exceeds 127.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL.	BIT. POS.	NAME	FUNCTION
			(m) 00001101 - Exponent Underflow Exception The final characteristic resulting from a floating-point arithmetic operation is less than zero. This interrupt is masked by E bit 38 of the current PSW).
			(n) 00001110 - Significance Exception The final fraction resulting from a floating-point addition or subtraction is equal to zero. This interrupt is masked by S (bit 39 of the current PSW).
			(o) 00001111 - Floating-Point Divide Exception The divisor fraction in a floating-point divide operation is equal to zero.
			Supervisor Call Level A Supervisor Call Interrupt occurs when a Supervisor Call (SVC) instruction is executed. When the Supervisor Call IIS occurs, the contents of the I field of the instruction are stored in the Interrupt Code. The hardware does not examine or modify this code. The Supervisor Call level interrupt cannot be masked. The ILC stored in the old PSW is 01_2, unless the SVC instruction is the subject instruction of an Execute instruction in which case the ILC is 10_2.

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
			(f) 00000110 - Specification Exception 1. The unit of information referenced is not on an appropriate boundary. 2. An invalid modifier field is specified in the STR instruction. 3. The R_1 field of an instruction which uses an even/odd pair of registers (64 bit operand) does not specify an even register. 4. A floating-point register other than 0, 2, 4, or 6 is specified. 5. A multiplicand or divisor in decimal arithmetic exceeds 15 digits and sign. 6. The first operand field is shorter than, or equal in length to, the second operand in decimal multiply and divide instructions. 7. The four low-order address bit specified by the contents of R_2 in a Set Storage Key or Insert Storage Key instruction are not equal to zero. (Feature F1622-00).

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
			8. The function specified by the I_2 field of a Diagnose instruction was not loaded in the transient area of control storage. 9. A Soft-Scope instruction (SSFS, SSRS) was issued without the supporting microcode loaded in the control storage transient area. (g) 00000111 - Data Exception 1. An invalid sign or digit code is detected in decimal operands. 2. Fields in decimal arithmetic overlap incorrectly. 3. The first operand of the Multiply Decimal instruction does not have a sufficient number of high-order zero digits. (h) 00001000 - Fixed-Point Overflow Exception A fixed-point add, subtract operation exceeds the capacity of the first operand field. This interrupt is masked by B (bit 36 of the current PSW).

Table 1-7. Interrupt Levels

Level	Interrupt
1	Processor Machine Check
2	Program Exception Level
3	Supervisor Call Level
4	Timer
5	I/O Status Tabler (IOST)
6	Monitor

Table 1-8. Interrupt Request Handling Priority Class

PRIORITY	PSW ADDRESS	INTERRUPT TYPE	CONTROLLED BY
1	03X	Proc, Machine Check	MACHINE CHECK LEVEL
2	04X	Program Exception	
3	05X	Supervisor Call	
4	-	Equipment Check	
5	-	IOST Machine Check	
6	06X	Interval Timer	System Mask
7	02X	IOST	System Mask
8	08X	Monitor Mode	PSW bit 19

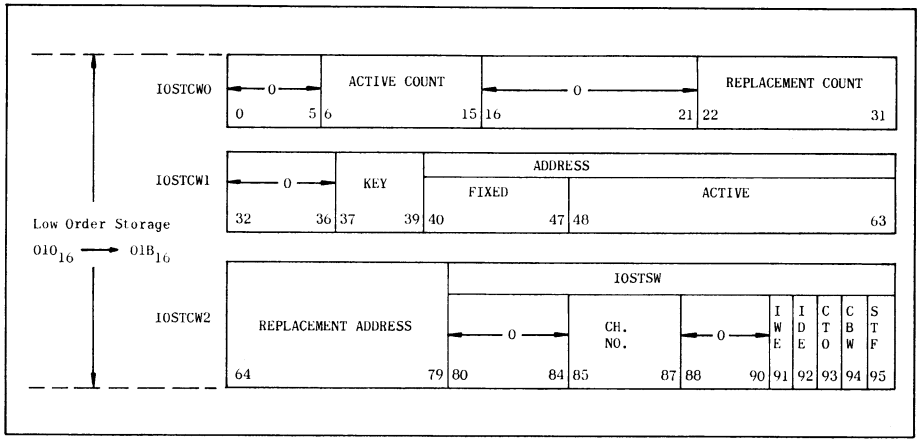

Figure 1-4. IOST Control Words

Table 1-5. Program Status Word Description (continued)

PSW FORMAT LEVEL	BIT POS.	NAME	FUNCTION
P R O G R A M M A S K	36 37 38 39	B D E S	NOTE Program Mask interrupts (bits 36-39) are active if set to 1 Fixed-point overflow mask Decimal overflow mask Exponent underflow mask Significance mask
I N S T R A D R S	40 to 63		Contains the address of the next instruction halfword in absolute form (loaded into IGRB 28 during PSW swap and converted to absolute address).

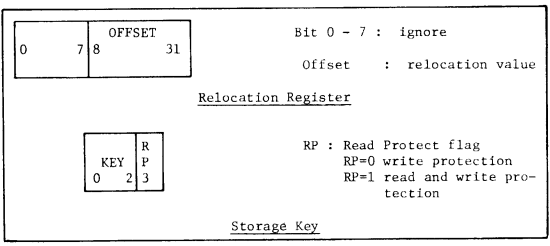

Figure 1-2. Relocation and Protection

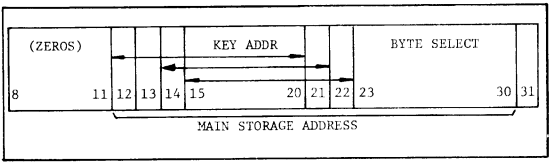

Figure 1-3. Key Address Format (Processor)

Table 1-6. Key Address Format (Processor)

Field/Bit (Refer to Fig. 1-3)	Description
Bits 8-11	Illegal storage address (should be zeros)
Bits 12-30	19-bit main storage address
Key Address	Key address portion of main storage
Bits 12-20	2048 Byte Block Protect
Bits 14-21	1024 Byte Block Protect
Bits 15-22	512 Byte Block Protect
Bit 31	Byte Select

Table 1-9. IOST Control Word Bit Assignment

Field/Bit (Ref. Fig. 1-4)	Description
(Bits 0-5)	Unassigned, must be set to zero.
Active Count (Bits 6-15)	The 10-bit count field specifies the number of words remaining in the status table. Decremented by one each time a status word is stored in the status table by the IOST. Maximum count is 1024 words specified by all zeroes.
(Bits 16-21)	Unassigned, must be set to zero.
Replacement Count (Bits 22-31)	The 10-bit count field which replaces the active count field when the active count is decremented to zero.
(Bits 32-36)	Unassigned, must be set to zero.
Key (Bits 37-39)	Contains the 3-bit storage protection key which is used by the IOST for all status table accesses. Unless the software replaces it at some later time, the key supplied in the initial IOSTCW will be used throughout the operation of the IOST. The key used for storage protection only addresses in the IOST is always absolute.
Address (Bits 40-63)	Contains the absolute address of the full word location in the status table area in storage where the next IOSTIW will be stored. The contents of the address field must be set up to point to the first (most significant) byte

Table 1-9. IOST Control Word Bit Assignment (continued)

Field/Bit (Ref. Fig 1-4)	Description
Address (Bits 40-63) (cont)	of the status table. The address must be on a full-word boundary or unpredictable status table entries will result.
Fixed (Bits 40-47)	Contains the fixed eight bit field of the status table address. No carry in will be premitted from the active field.
Active (Bits 48-63)	This address is incremented by 4 after each IOSTIW is stored. This field will be replaced by the replacement address when the active count is decremented to zero. This field will point to the most significant byte of the next IOSTIW location.
Replacement Address (Bits 64-79)	This address will be written into the active portion of the address field (Bits 48-63) when the active count steps to zero.
IOSTSW (Bits 80-95)	IOST Status Word (IOSTSW): contains any error conditions encountered by the IOST in attempting to store status in the status table.
(Bits 80-84)	Set to zero.
CH. NO. (Bits 85-87)	Channel Number: contains the number of the selected channel being serviced by the IOST when an error condition occurred.
(Bits 88-90)	Unassigned, must be set to zero.

Table 1-9. IOST Control Word Bit Assignment (continued)

Field/Bit (Ref. Fig. 1-4)	Description
IWE (Bit 91)	Interrupt Word Error: a protection exception or addressing exception error was detected by the IOST when it attempted to read or write an IOSTIW from or into the status table or to read a BCSW. The IOSTIW to be stored is saved in the BCSW in low order main storage location OEO_{16} through OEF_{16}.
IDE (Bit 92)	Interrupt Data Error: an address check or data parity check error was detected by the IOST when it attempted to read or write an IOSTIW from or into the status table or to read a BCSW. The IOSTIW to be stored is saved in the BCSW in low order main storage location OEO_{16} through OEF_{16}.
CTO (Bit 93)	Channel Time Out: the CTO bit is set when the selected channel fails to respond to the Status Service Request Acknowledge (SSRA) signal within the specified time. The contents of the addressed location where the IOSTIW was to be stored are unpredictable.

Table 1-9. IOST Control Word Bit Assignment (continued)

Field/Bit (Ref. Fig. 1-4)	Description
CBW (Bit 94)	Channel Buffer Word error: an error (i.e. addressing exception, protection exception, address check, write bus check) was detected by the selected channel when it attempted to write its IOSTIW into the BCSW storage location. The contents of the BCSW is unpredictable.
STF (Bit 95)	Status Table Full: The IOST detected a V-bit set to zero at the status table location where the IOSTIW was to be stored, indicating a full status table. The IOSTIW to be stored is saved in the BCSW location.

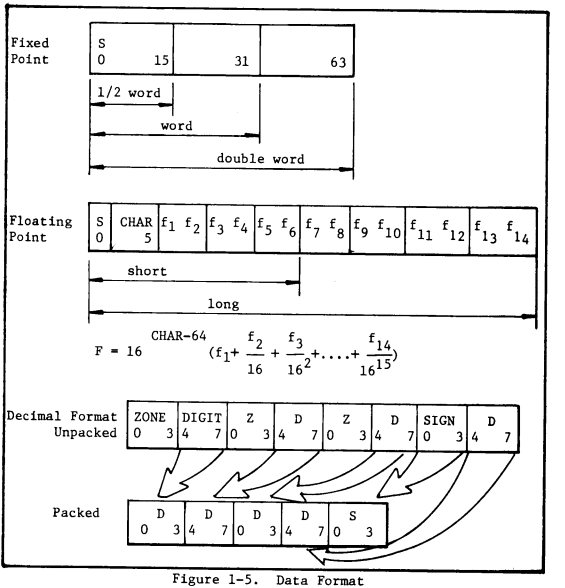

Figure 1-5. Data Format

Table 1-10. Decimal Data Code

EBCDIC 16	ASCII 16	
A+	A+	Sign
B-	B-	
*C+	*C+	
*D-	*D-	
E+	E+	
F+	F+	
*F	*3	Zone

*Processor generated.

Table 1-11. OP Code, Mnemonic Code

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0				03 P STR RR	04 SPM RR	05 BALR RR	06 BCTR RR	07 BCR RR	08FP SSK RR	09FP ISK RR	0A SVC RR			0D I BASR RR		
1	10 F LPR RR	11 LNR RR	12 LTR RR	13 LCR RR	14 NR RR	15 CLR RR	16 OR RR	17 XR RR	18 LR RR	19 CR RR	1A AR RR	1B SR RR	1C F MR RR	1D F DR RR	1E F ALR RR	1F F SLR RR
2	20 F LPDR RR	21 F LNDR RR	22 F LTDR RR	23 F LCDR RR	24 F HDR RR				28 F LDR RR	29 F CDR RR	2A F ADR RR	2B F SDR RR	2C F MDR RR	2D F DDR RR	2E F AWR RR	2F F SWR RR
3	30 F LPER RR	31 F LNER RR	32 F LTER RR	33 F LCER RR	34 F HER RR				38 F LER RR	39 F CER RR	3A F AER RR	3B F SER RR	3C F MER RR	3D F DER RR	3E F AUR RR	3F F SUR RR
4	40 STH RX	41 LA RX	42 STC RX	43 IC RX	44 EX RX	45 BAL RX	46 BCT RX	47 BC RX	48 LH RX	49 CH RX	4A AH RX	4B SH RX	4C MH RX	4D I BAS RX	4E CVD RX	4F CVB RX
5	50 ST RX				54 N RX	55 CL RX	56 O RX	57 X RX	58 L RX	59 C RX	5A A RX	5B S RX	5C M RX	5D D RX	5E F AL RX	5F F SL RX
6	60 F STD RX								68 F LD RX	69 F CD RX	6A F AD RX	6B F SD RX	6C F MD RX	6D F DD RX	6E F AW RX	6F F SW RX

Table 1-11. OP Code, Mnemonic Code (continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
7	70 F STE RX								78 F LE RX	79 F CE RX	7A F AE RX	7B F SE RX	7C F ME RX	7D F DE RX	7E F AU RX	7F F SU RX
8	80 P SSM SI		82 P LPSW SI	83 P DIAG SI			86 F BXH RS	87 F BXLE RS	88 SRL RS	89 SLL RS	8A F SRA RS	8B F SLA RS	8C F SRDL RS	8D F SLDL RS	8E F SRDA RS	8F F SLDA RS
9	90 STM RS	91 TM SI	92 MVI SI	93 F TS SI	94 NI SI	95 CLI SI	96 OI SI	97 XI SI	98 LM SI	99 P HPR SI	9A AI SI		9C P SIO SI			
A			A2 P SSFS RS	A3 P SSRS RS			A6 U AI SI				AA U AH RX	AB U SH RX				
B	B0 P SSTM RS	B1 P LCS RS							B8 P SLM RS							
C																
D		D1 MVN SS	D2 MVC SS	D3 MVZ SS	D4 NC SS	D5 CLC SS	D6 OC SS	D7 XC SS					DC TR SS	DD TRT SS	DE ED SS	DF F EDMK SS

Table 1-11. OP Code, Mnemonic Code (continued)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E																
F		F1 MVO SS	F2 PACK SS	F3 UNPK SS					F8 ZAP SS	F9 CP SS	FA AP SS	FB SP SS	FC MP SS	FD DP SS		

NOTES FOR TABLE 1-11:

1. First line : OP Code
2. Second line : MNEMONIC Code
3. Third line : Format Type

"P" Privileged instruction

"F" Feature instruction

"U" 92/9300 Mode only

"I" 360/20 Mode only

REVISION: HCB-2

COMPANY CONFIDENTIAL

IH12438

Table 1-12. Symbols and Abbreviations

Symbol	Definition
OP. CODE	Instruction operation code
COMP.	Compatibility
I	360/20 compatibility instruction
U	92/9300 compatibility instruction
Ⓘ	360/20 mode only
Ⓤ	92/9300 mode only
PRIV. /F.	Privileged instruction and Feature instruction
MNEM. CODE	Mnemonic code
INST. NAME	Instruction name
CC	Condition code
OPERATION	
R1-R3	General register number that contains operand 1-3.
X2	General register number that contains an index number for operand 2 of an RX instruction.
I2	Immediate operand OC indirection
L	One less than length of operand 1 and 2
L1(L2)	One less than length of operand 1 (2)
B1(B2)	General register that contains base address of operand 1 (2).
D1(D2)	Displacement value for base address of operand 1 (2)
+	Add
-	Subtract
x	Multiply
÷	Divide
Ⓞor	Logical "OR"
Ⓧxor	Logical "Exclusive OR"
Ⓐ	Logical "AND"
:	Compare
PROG. EXCP	
PX	Protection exception
AX	Address exception
SPX	Specification exception
DX	Data exception
OX	Operation exception
POX	Privileged operation exception
FPOX	Fixed point overflow exception
FPDX	Fixed point divide exception
DOX	Decimal overflow exception
DDX	Decimal divide exception
EOX	Exponent overflow exception
EUX	Exponent underflow exception
SIGX	Significance exception
FLPDX	Floating point divide exception
EX	Execute exception
2	Used to indicate second operand in condition codes.

Table 1-13. Instruction Repertoire

RR	OP CODE 0 7	R1 8 11	R2 12 15

OP CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PFX	AFX	SPX	DFX	XOX	POX	FPDX	FPOX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EFX
03		P	STR	SERV. TIMER REG.	OP CODE, R1, OCLS L=0 ITR→R1, C=0ITR→R1, L=1 R1→ITR, C=1ITR→R1, S=0 TURN ON S=1 TURN OFF	0	P		R			x			x									
04			SPM	SET PROG. MASK	$R1_{2-7} \rightarrow PSW_{34-39}$	(R1 bit 2,3)																		
05			BALR	BRANCH AND LINK	$PSW_{32-39} \rightarrow R1_{0-7}$, B28-B29 $\rightarrow R1_{8-31}$, R2-PSW(B28)																				
06			BCTR	BRANCH ON COUNT	IF R1-1≠0, R2→PSW(B28)																				
07	I		BCR	BRANCH ON COND.	IF M1=CC, R2→PSW(B28)																				
08		P.F	SSK	SET STOR.KEY	$R1_{25-28} \rightarrow$ KEY MEM. ($R2_{8-21}$)						x	x		x	x									
09		P.F	ISK	INSERT STOR. KEY	KEY MEM ($R2_{8-21}$) $\rightarrow R1_{25-28}$						x	x		x	x									

REVISION: HCB-2

COMPANY CONFIDENTIAL

Table 1-13. Instruction Repertoire (cont)

RR

OP CODE	R1	R2
0 7	8 11	12 15

OP CODE	COMP.	PRIV. /F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FP OX	FP DX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
0A			SVC	SUPRV.CALL	GEN.INT.REQ. I1→PSW$_{24-31}$	(New PSW)																		
0D	(1)		BASR	BRANCH AND STORE	B28-B29+R1$_{16-31}$ R2→PSW(B28)																			
10		F	LPR	LOAD POS.	R2(+)→R1, $\overline{R2(-)}$→R1	=0		>0	0V					x		x								
11		F	LNR	LOAD NEG.	R2(-)→R1, $\overline{R2(+)}$→R1	=0	<0							x										
12			LTR	LOAD AND TEST	R2→R1	=0	<0	>0																
13		F	LCR	LOAD COMPL.	R2→R1	=0	<0	>0	0V					x		x								
14			NR	AND	R1 ⊙ R2→R1	=0	<0																	
15			CLR	COMP. LOGICAL	R1 : R2	=2	<2	>2																
16			OR	OR	R1 ⊕ or R2→R1	=0	<0																	
17			XR	EX.OR	R1 ⊕ xor R2→R1	=0	>0																	
18			LR	LOAD	R2→R1																			

Table 1-13. Instruction Repertoire (cont)

RR

OP CODE	R1	R2
0 7	8 11	12 15

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
19			CR	COMP.	R1 : R2	=2	<2	>2																
1A	I		AR	ADD	R1+R2→R1	=0	<0	>0	OV							x								
1B	I		SR	SUBT.	R1−R2→R1	=0	<0	>0	OV							x								
1C		F	MR	MULT.	R1 x R2→R1							x		x										
1D		F	DR	DIV.	R1 ÷ R2→R1							x		x			x							
1E		F	ALR	ADD LOG.	R1+R2→R1	=0	≠0	=0	≠0					x										
1F		F	SLR	SUBT. LOG.	R1−R2→R1		≠0	=0	≠0					x										
20		F	LPDR	LOAD POS. LONG	R2(2W)→R1(2W), SIGN +	=0		>0			x		x											
21		F	LNDR	LOAD NEG. LONG	R2(2W), SIGN −	=0	<0					x		x										
22		F	LTDR	LOAD AND TEST L.	R2(2W)→R1(2W)	=0	<0	>0				x		x										

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Table 1-13. Instruction Repertoire (cont)

RR

OP CODE		R1		R2	
0	7	8	11	12	15

OP. CODE	COMP	PRIV./F	MENM. CODE	INST. NAME	OPERATION	CC 00	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
23		F	LCDR	LOAD COMPL.L.	R2(2W)→R1(2W), Sign is reversed.	=0	<0	>0				x		x										
24		F	HDR	HALVE L.	R2(2W) : 2→R1(2W)							x		x							x			
28		F	LDR	LOAD L.	R2(2W)→R1							x		x										
29		F	CDR	COMP.L.	R2(2W):R1(2W)	=2	<2	>2				x		x										
2A		F	ADR	ADD NORM.L.	R1(2W)+R2(2W)→R1(2W)	=0	<0	>0				x		x						x	x	x		
2B		F	SDR	SUBT.L.	R1(2W)-R2(2W)→R1(2W)	=0	<0	>0				x		x						x	x	x		
2C		F	MDR	MULT.L.	R1(2W)xR2(2W)→R1(2W)							x		x						x	x			
2D		F	DDR	DIV.L.	R1(2W)÷R2(2W)→R1(2W), no remainder	=0	<0	>0				x		x						x	x		x	
2E		F	AWR	ADD UNNORM.L.	R1(2W)+R2(2W)→R1(2W)	=0	<0	>0				x		x						x		x		
2F		F	SWR	SUL.UNNORM.L.	R1(2W)-R2(2W)→R1(2W)	=0		>0				x		x						x		x		
30		F	LPER	LOAD POS. SHORT	R2(W)→R1(W), SIGN +							x		x										

Table 1-13. Instruction Repertoire (cont)

RR

OP CODE	R1	R2
0 7	8 11	12 15

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	TPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
31		F	LNER	LOAD NEG. SHORT	R2(W)→R1(W), SIGN -	=0	<0					x		x										
32		F	LTER	LOAD AND TEST S.	R2(W)→R1(W)	=0	<0	>0				x		x										
33		F	LCER	LOAD COMPL.S.	R2(W)→R1(W), Sign is reversed.	=0	<0	>0				x		x										
34		F	HER	HALVE S.	R2(W)÷2→R1(W)							x		x							x			
38		F	LER	LOAD S.	R2(W)→R1(W)							x		x										
39		F	CER	COMP. S.	R2(W):R1(W)	=2	<2	>2				x		x										
3A		F	AER	ADD NORM.S.	R1(W)+R2(W)→R1(W)	=0	<0	>0				x		x						x	x	x		
3B		F	SER	SUB.NORM.S.	R1(W)-R2(W)→R1(W)	=0	<0	>0				x		x						x	x	x		
3C		F	MER	MULT.S.	R1(W)xR2(S)→R1(2W)							x		x						x	x			
3D		F	DER	DIV.S.	R1(W)÷R2(W)→R1(W), no remainder.							x		x						x	x		x	

Table 1-13. Instruction Repertoire (cont)

RR	OP CODE 0		7	R1 8	11	R2 12	15																			
OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	1	2	3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	PDX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
3E	F	AUR	ADD UNNORM. S.	R1(W)+R2(W)→R1(W)	=0	<0	>0				x		x							x		x		
3F	F	SUR	SUB.UNNORM. S.	R1(W)−R2(W)→R1(W)	=0	<0	>0				x		x							x		x		

Table 1-13. Instruction Repertoire (cont)

RX

OP CODE	R1	X2	B2	D2
0 7	8 11	12 15	16 19	20 31

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
40	IU		STH	STORE 1/2 W.	$R1_{16-31} \rightarrow X2B2D2$					x	x	x												
41			LA	LOAD ADDR.	$X2B2D2 \rightarrow R1_{8-31}$																			
42			STC	STORE CH.	$R1_{24-31} \rightarrow X2B2D2$					x	x															
43			IC	INSERT CH.	$(X2B2D2) \rightarrow R1_{24-31}$					x	x															
44			EX	EXECUTE	INSTR.AT(X2B2D2), modified by $R1_{24-31}$	Set by subj. instr.				x	x	x														x
45	U		BAL	BRANCH AND LINK	$PSW_{32-39} \rightarrow R1_{0-7}$, B28-B29 $\rightarrow R1_{8-31}$, $X2B2D2 \rightarrow PSW$																					
46			BCT	BRANCH ON COUNT	IF R1-1≠0, $X2B2D2 \rightarrow PSW$																					
47	IU		BC	BRANCH ON COND.	IF M1=CC, $X2B2D2 \rightarrow PSW$																					
48	IU		LH	LOAD 1/2 W.	$(X2B2D2)(1/2W) \rightarrow R1(W)$					x	x	x														

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Table 1-13. Instruction Repertoire (cont)

RX

OP CODE		R1		X2		B2		D2	
0	7	8	11	12	15	16	19	20	31

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
49	IU		CH	COMP.1/2W.	R1(W):(X2B2D2)(1/2W)	=2	<2	>2		x	x	x												
4A	I		AH	ADD 1/2W.	(X2B2D2)(1/2W)+R1(W) →R1(W)	=0	<0	>0	OV	x	x	x				x								
4B	I		SH	SUBT.1/2W.	R1(W)-(X2B2D2)(1/2W) →R1(W)	=0	<0	>0	OV	x	x	x				x								
4C			MH	MULT.1/2W.	R1(W)×(X2B2D2)(1/2W) →R1(W)					x	x	x		x										
4D	(I)		BAS	BRANCH AND STORE	B28-B29→R1$_{16-31}$, B2D2→PSW																			
4E			CVD	CONV. TO DEC.	R1(W)→X2B2D2(2W), packed decimal.					x	x	x												
4F			CVB	CONV. TO BIN.	(X2B2D2)(2W)→R1(W), binary					x	x	x	x				x							
50			ST	STORE	R1→X2B2D2					x	x	x												
54			N	AND	R1 ⊙ (X2B2D2)→R1	=0	≠0			x	x	x												

Table 1-13. Instruction Repertoire (cont)

RX

OP CODE	R1	X2	B2	D2
0 /	8 11	12 15	16 19	20 31

OP CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
55			CL	COMP.LOG.	R1:(X2B2D2)	=2	<2	>2		x	x	x												
56			O	OR	R1 ⊕or (X2B2D2)→R1	=0	≠0			x	x	x												
57			X	EX. OR	R1 ⊕xor (X2B2D2)→R1	=0	≠0			x	x	x												
58			L	LOAD	(X2B2D2)→R1					x	x	x												
59			C	COMP.	R1:(X2B2D2)	=2	<2	>2		x	x	x												
5A			A	ADD	R1+(X2B2D2)→R1	=0	<0	>0	OV	x	x	x				x								
5B			S	SUBT.	R1-(X2B2D2)→R1	=0	<0	>0	OV	x	x	x				x								
5C			M	MULT.	R1x(X2B2D2)→R1(2W)					x	x	x												
5D			D	DIV.	R1(2W):(X2B2D2)(W)→R1					x	x	x					x							
5E		F	AL	ADD LOG.	R1+(X2B2D2)→R1	=0	≠0	=0	≠0	x	x	x		x										
5F		F	SL	SUBT.LOG.	R1 (X2B2D2)→R1		≠0	=0	≠0	x	x	x		x										
60		F	STD	STORE LONG	R1(2W)→X2B2D2(2W)					x	x	x		x										

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Table 1-13. Instruction Repertoire (cont)

RX	OP CODE			R1		X2		B2		D2	
	0		7	8	11	12	15	16	19	20	31

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
68		F	LD	LOAD L.	(X2B2D2)(2W)→R1(2W)					x	x	x		x									
69		F	CD	COMP. L.	(X2B2D2)(2W):R1(2W)	=2	<2	>2		x	x	x		x									
6A		F	AD	ADD NORM.L.	R1(2W)+(X2B2D2)(2W) →R1(2W)	=0	<0	>0		x	x	x		x					x	x	x		
6B		F	SD	SUBT.NORM.L.	R1(2W)-(X2B2D2)(2W) →R1(2W)	=0	<0	>0		x	x	x		x					x	x	x		
6C		F	MD	MULT.L.	R1(2W)x(X2B2D2)(2W) →R1(2W)					x	x	x		x					x	x			
6D		F	DD	DIV.L.	R1(2W):(X2B2D2)(2W) →R1(2W)					x	x	x		x					x	x		x	
6E		F	AW	ADD UNNORM. L.	R1(2W)+(X2B2D2)(2W) →R1(2W)	=0	<0	>0		x	x	x		x					x		x		
6F		F	SW	SUBT.UNNORM. L.	R1(2W)-(X2B2D2)(2W) →R1(2W)	=0	<0	>0		x	x	x		x					x		x		
70		F	STE	STORE SHORT	R1(W)→X2B2D2(W)					x	x	x		x									

Table 1-13. Instruction Repertoire (cont)

RX	OP CODE		R1		X2		B2		D2	
	0	7	8	11	12	15	16	19	20	31

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS: PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
78			LE	LOAD S.	(X2B2D2)(W)→R1(W)					x	x	x		x										
79		F	CE	COMP.SHORT	R1(W):(X2B2D2)(W)	=2	<2	>2		x	x	x		x										
7A		F	AE	ADD NORM.S.	R1(W)+(X2B2D2)(W)→R1(W)	=0	<0	>0		x	x	x		x						x	x	x		
7B		F	SE	SUBT.NORM.S.	R1(W)-(X2B2D2)(W)→R1(W)	=0	<0	>0		x	x	x		x						x	x	x		
7C		F	ME	MULT.S.	R1(W)x(X2B2D2)(W)→R1(2W)					x	x	x		x						x	x			
7D		F	DE	DIV.S.	R1(W):(X2B2D2)(W)→R1(W)					x	x	x		x						x	x		x	
7E		F	AU	ADD UNNORM. S.	R1(W)+(X2B2D2)(W)→R1(W)	=0	<0	>0		x	x	x		x						x		x		
7F		F	SU	SUBT.UNNORM. S.	R1(W)-(X2B2D2)(W)→R1(W)	=0	<0	>0		x	x	x		x						x		x		

REVISION: HCB-2

COMPANY CONFIDENTIAL

Table 1-13. Instruction Repertoire (cont)

RS	OP CODE	R1	B2	D2	
SI	OP CODE	I2	B1	D1	
	0 7	8 15	16 19	20 31	

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
80		P	SSM	SET SYST. MASK(S1)	$(B1D1)_{0-7} \rightarrow PSW_{0-7}$					x	x	x			x									
81	I		SPSW		Not valid																			
82		P	LPSW	LOAD PSW(SI)	(B1D1)(2W)→PSW, IF I2=01 inhibit int.	(l o a d e d)				x	x	x			x									
83	I		DIAG		Not valid																			
83		P	DIAG	DIAGNOSE(SI)	$I2=00_{16}$ SYS.RESET, B1D1 is ignored.							x			x									
86		F	BXH	BRANCH ON INDEX H	IF R1 + R3 >R3 or R3 + 1 (ODD REG), B1D1→PSW									x										
87		F	BXLE	BRANCH ON INDEX LE	IF R1 + R3 ≤R3 or R3 + 1 (ODD REG), B1D1→PSW									x										
88			SRL	SHIFT R.S. LOG.	R1(W) SR (B2D2 LOW-ORDER 6 BIT)																			

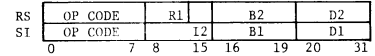
Table 1-13. Instruction Repertoire (cont)

| | | |

Table 1-13. Instruction Repertoire (cont)

| | | |

Table 1-13. Instruction Repertoire (cont)



OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
99	I		HPR		Not valid																			
9A			AI	ADD IMMED. (SI)	(B1D1)(1/2W)+I_2(1/2W) →B1D1(1/2W)	=0	<0	>0	OV	x	x	x				x								
9A	I		TIOB		Not valid																			
9B	I		CIO		Not valid																			
9C		P	SIO	START I/O (SI)	B1D1→BIT 21-23=CH#, BIT24-31=DEV# CC=0 ACCEPT CC=2 BUSY CC=1 REJECT CC=3 NOT OPERATIONAL	(depends on channel)									x									
A0	U		SPSC		Not valid																			
A1	U		SRC		Not valid																			
A2		P	SSFS	SOFT-SCOPE F.S.	See Note 1					x	x	x			x									

Table 1-13. Instruction Repertoire (cont)

RS	OP CODE	R1		B2	D2
SI	OP CODE		I2	B1	D1
	0 7	8 15	16 19	20 31	

OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	FOX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
A3		P	SSRS	SOFT-SCOPE R.S.	See Note 2					x	x	x			x									
A4	U		XIOF		Not valid																			
A5	U		TIO		Not valid																			
A6	(U)		AI	ADD IMMED.	I2 + (B1D1)→B1D1																			
A8	U		LPSC		Not valid																			
A9	U		HPR		Not valid																			
AA	(U)		AH	ADD H. (RX)	RI + (B2D2)(1/2W)→R1(W)	=0	<0	>0	OV	x	x	x				x								
AB	(U)		SH	SUBT.H.(RX)	R1 - (B2D2)(1/2W)→R1(W)	=0	<0	>0	OV	x	x	x				x								
B0		P	SSTM	SUPV. STORE MULT.	R1 THRU R3→B2D2(R1,R3= PROB.REG.)					x	x	x			x									

Table 1-13. Instruction Repertoire (cont)

RS	OP CODE	R1		B2	D2
SI	OP CODE		I2	B1	D1
	0 7	8 15	16 19	20 31	

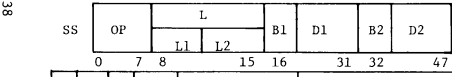
OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
B1		P	LCS	LOAD C.S.	(B2D2)→C.S. R1=Hash total *CC=0 data transfer incomp. CC=1 data transfer comp. CC=3 Hash total error					x	x	x			x									
B8		P	SLM	SUPV. LOAD MULT.	(B2D2)→R1 THRU R3 (R1,R3=PROB.REG.)					x	x	x			x									

REVISION: HCB-2

COMPANY CONFIDENTIAL

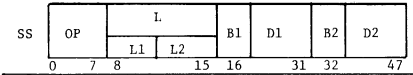
M12438

Table 1-13. Instruction Repertoire (cont)



OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
D0	I		XIO		Not valid																			
D1	IU		MVN	MOVE NUMERIC	(B2D2) NUM.→B1D1					x	x													
D2	IU		MVC	MOVE	(B2D2)→B1D1					x	x													
D3	I		MVZ	MOVE ZONE	(B2D2) ZONE→B1D1					x	x													
D4	U		NC	AND	(B2D2) $\odot$ (B1D1)→B1D1	=0	≠0			x	x													
D5	IU		CLC	COMP.LOG.	(B1D1):(B2D2)	=2	<2	>2		x	x													
D6	U		OC	OR	(B1B1) $\oplus$or (B2D2)→B1D1	=0	≠0			x	x													
D7			XC	EX. OR	(B1D1) $\oplus$xor(B2D2)→B1D1	=0	≠0			x	x													
DC	IU		TR	TRANSLATE	(B1D1)+B2D2 →B1D1					x	x													

Table 1-13. Instruction Repertoire (cont)

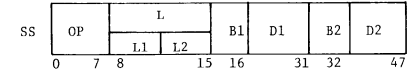


OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
DD			TRT	TRANSL. AND TEST	IF{(B1D1)+B2D2}=all zero ignore and continue IF{(B1D1)+B2D2}=none-zero argument address →GEN.REG.1 result byte→GEN.REG.2 *CC=0 all result bytes are zero. CC=1 non-zero byte is not last byte. CC=2 non-zero byte is last byte.					x	x													
DE	IU		ED	EDIT	UNPACK (B2D2)→EDIT →B1D1	0	-	+		x	x		x												

REVISION: HCB-2

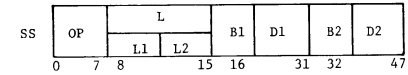
COMPANY CONFIDENTIAL

Table 1-13. Instruction Repertoire (cont)



OP. CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
DF		F	EDMK	EDIT AND MARK	UNPACK (B2D2)→EDIT →B1D1 Addr.of first significant char- acter→GEN.REG.1	0	-	+		x	x		x	x				x						
F1	IU		MVO	MOVE WITH OFFSET	L2(B2D2)→SHIFT LEFT 4 BIT→L1(B1D1)					x	x													
F2	IU		PACK	PACK	L2(B2D2)→PACK→L1(B1D1)					x	x													
F3	IU		UNPK	UNPACK	L2(B2D2)→UNPACK →L1(B1D1)					x	x													
F8	IU		ZAP	ZERO AND ADD	L2(B2D2) + 0→L1(B1D1)	=0	<0	>0	OV	x	x		x					x						
F9	IU		CP	COMP. DECIMAL	L2(B2D2):L1(B1D1)	=2	<2	>2			x		x	x										
FA	IU		AP	ADD DEC.	L1(B1D1)+L2(B2D2) →L1(B1D1)	=0	<0	>0	OV	x	x		x					x						

Table 1-13. Instruction Repertoire (cont)



OP CODE	COMP.	PRIV./F	MNEM. CODE	INST. NAME	OPERATION	CC 0	CC 1	CC 2	CC 3	PROGRAM EXCEPTIONS PX	AX	SPX	DX	OX	POX	FPOX	FPDX	DOX	DDX	EOX	EUX	SIGX	FLPDX	EX
FB	IU		SP	SUBT.DEC.	L1(B1D1)-L2(B2D2) →L1(B1D1)	=0	<0	>0	OV	x	x		x					x						
FC	IU		MP	MULT.DEC.	L1(B1D1)xL2(B2D2) →L1(B1D1),L1>L2					x	x	x	x												
FD	IU		DP	DIV.DEC.	L1(B1D1)+L2(B2D2) →L1(B1D1)					x	x	x	x						x						

REVISION: HCB-2

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Table 1-13. Instruction Repertoire (cont)
Notes 1 and 2

	OP CODE 0 7	R1 8 11	R3 12 15	SYNC SEL 16 19	SYNC TEST 20 23	NOT USED 24 27	S BUS SELECT 28 31
NOTE 1:	A2-SSFS	SUPERVISOR GEN. REG.	SUPERVISOR GEN. REG.	SELECT SIGNAL TO SYNC ON.	DETERMINES POLARITY TO SYNC ON.		SELECTS BUS TO SAMPLE FROM
NOTE 2:	A3-SSRS	NO. OF SAMPLES TO TAKE	ABSOLUTE STARTING ADDRESS FOR SOFTSCOPE SCANNED DATA	ONLY FOUR MOST SIGNI-FICANT BITS OF BUS SELECTED USED.	1 = HIGH 0 = LOW		0 0 0 1-BUS 1,0717 RDR. 0 0 1 0-BUS 2, NOT USED 0 0 1 1-BUS 3,0773 PTR. 0 1 0 0-BUS 4,IDA 0 1 0 1-BUS 5,DISK DRIVES 0 1 1 0-BUS 6,0605 PUNCH (P) 0 1 1 1-BUS 7,0605 PUNCH (R)
		SCAN RATE BETWEEN SAMPLES		0 1 2 3			
		INITIAL DELAY BETWEEN SYNC & DATA SAMPLE		1 0 0 0=8-BIT 0 0 1 0 0=4-BIT 1 0 0 1 0=2-BIT 2 0 0 0 1=1-BIT 3 0 0 0 0=0-U.C.			

SSFS (SOFTSCOPE FORWARD SCAN): CC=0 SYNC DETECTED
CC=3 SYNC NOT DETECTED

SSRS (SOFTSCOPE REVERSE SCAN): CC=0 SYNC DETECTED ON FIRST BUFFER ITERATION
CC=1 SYNC NOT DETECTED ON FIRST BUFFER ITERATION
CC=2 SYNC DETECTED ON SUBSEQUENT ITERATIONS
CC=3 SYNC NOT DETECTED ON SUBSEQUENT ITERATIONS

SSFS AND SSRS ARE PRIVELEDGED INSTRUCTIONS.

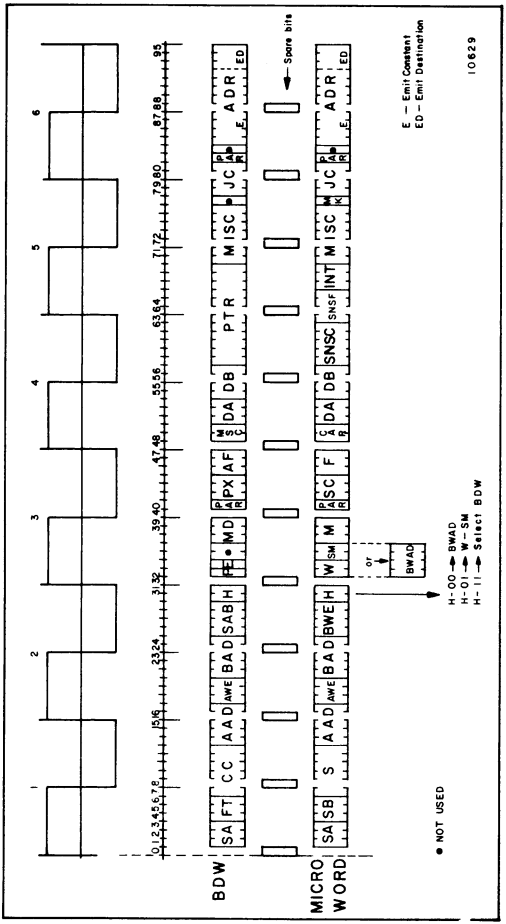

Figure 1-6. Microword Format

Table 1-14. Microinstruction Format

Position	Field	Bits	Description
1	SA	3	Select A Input to Shifter
2	*SB	3	Select B Input to Shifter
3	*S	5	Shift Control
4	AAD	4	IGR A Address
5	AWE	3	IGR A Write Enable (Byte Select)
6	BAD	4	IGR B Read Address
7	*BWE	4	IGR B Write Enable (Byte Select)
8	H	2	Format Control: Selects BWAD or W and SM Fields.
9	*BWAD	4	IGR B Write Address (overlays W and SM Fields)
(9ab)	*W	(2)	Load WDR (Write Data Register)
(9c)	*SM	(2)	Input to MAR (Memory Address Register)
10	*M	3	Main Store Control
11	*SC	3	Input to C Register
12	*F	3	Adder Function
13	*CAR	2	Carry into Adder
14	DA	3	A Operand
15	DB	3	B Operand
16	*SNSC	5	Sense Condition
17	*SNSF	3	Sense Destination Flip-Flop
18	*INT	3	Interrupt Control
19	MISC	6	Miscellaneous Controls
20	*MK	1	Mark Control
21	JC	3	Jump Control
22	PTY	2	Parity Bits
23	Spare	1	Not used
24	ADDR	11	Jump Address(overlays E and ED fields)
(24a)	E	(8)	Emit Constant
(24b)	ED	(3)	Emit Destination

NOTE: *These fields are not available in the BDW microinstruction.

Table 1-15. BDW Microinstruction Format

Position	Field	Bits	Description
1	SA	3	Select A Input to Shifter
2	*FT	3	Feature required 000 no special feature required 001 Microinstruction Expansion feature 010 undefined 011 Storage Protect feature 100 undefined 101 undefined 110 undefined 111 undefined
3	*CC	5	Condition Code grouping (See Table 1-28)
4	AAD	4	IGR A Address
5	AWE	3	IGR A Write Enable (Byte Select)
6	BAD	4	IGR B Read Address
7	*SAB	4	Sense and Branch grouping (3 Bits and 1 Future)(See tables 1-15 thru 1-23 & 1-29)
8	H	2	Format Control: selects BDW format
9a	*P	1	Privileged bit 0 - not privileged 1 - privileged, causes privileged exception interrupt if not in privileged mode.
9b	*E	1	Execute bit 0-not execute instruction 1-execute instruction (EX)
9c	*Future	2	Not used.
10	*MD	3	Mode validation bits 000 - invalid in all modes 1xx - valid in 90/30 mode x1x - valid in 360/20 mode xx1 - valid in 9200/9300 mode 111 - valid in all modes
11	*PX	3	Program Exception group (INT) (2 Bits and 1 Future)(See table 1-30)
12	*AF	3	Adder function called by OPC (101) when specified by F field. 000 - Binary Add 001 - Binary Subtract (twos complement) 010 - Logical AND 011 - Inclusive OR 100 - Exclusive OR 101 - undefined 110 - Decimal Subtract (nines complement) 111 - undefined

Table 1-15. BDW Microinstruction Format (cont)

Position	Field	Bits	Description
13	*MSC	2	Miscellaneous functions grouping (See Table 1-26)
14	DA	3	A Operand
15	DB	3	B Operand
16-18	*PTR	11	Pointer loaded into Mark register (jump to Mark register at end of staticize)
19	MISC	6	Miscellaneous Controls (See table 1-26)
20	*Future	1	Not used
21	JC	3	JUMP Control
22	PTY	2	Parity Bits
23	Spare	1	Not Used
24	ADDR	11	Jump Address (overlays E and ED fields)
(24a)	E	(8)	Emit Constant
(24b)	ED	(3)	Emit Destination

NOTE: *These fields are unique to the BDW microinstruction format.

Table 1-16. Sense and Branch Group Ø

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
000	00000	IXEQ0	I12-15 = 0 + PSW16-18 = 001 (92-9300 MODE)
000	00001	P1618EQ2	PSW16-18 = 010 (360/20 MODE)
000	00010	TIRQ	INTERVAL TIMER INTERRUPT REQUEST
000	00011	ZBEQ0	Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 OR 010))
000	00100	EXEC	EXECUTE FF = 1
000	00101	NITASC	SYNCHFF = 1 * NO INTERVAL TIMER INTERRUPT REQUEST
000	00110	BCNTNEQ0	(L00-31 = NONZERO) * (I01 = 1 + I12-15 = NONZERO)
000	00111	P1618EQ0	PSW16-18 = 000 (NATIVE MODE)
000	01000	IR2NEQ0	I12-15 = NONZERO (R2 NONZERO)
000	01001	L1631EQ0	L16-31 = 0
000	01010	I07EQ1	I07 = 1
000	01011	Z00EQ1	Z00 = 1
000	01100	Z01EQ1	Z01 = 1
000	01101	ONE	1 (+5V.)

Table 1-16. Sense and Branch Group Ø (cont)

Current BDW / SAB Field (Bits 1,2,3)	Current Microinstruction NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
000	01110	IOSTER	IOST11-15 = NONZERO (IOST ERROR)
000	01111	Z0615EQ1	Z06-15 = 1
000	10000	IR1EQ0	I08-11 = 0 (R1 = 0)
000	10001	Z0001NEQ0	Z00-01 = NONZERO
000	10010	LEQ0	L00-31 = 0
000	10011	ISS0PEX	(I00-03=F+D) *OPERATION EXCEPTION
000	10100		
000	10101		
000	10110		
000	10111		

Table 1-17. Sense and Branch Group 1

Current BDW / SAB Field (Bits 1,2,3)	Current Microinstruction NOTE Conditions are called by SAFE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
001	00000	I05EQ1	I05 = 1
001	00001	I07EQ0	I07 = 0
001	00010	I07EQ1	I07 = 1
001	00011	I03EQ1	I03 = 1
001	00100	P39EQ1	PSW39 = 1 SIGNIFICANCE MASK BIT
001	00101	I06EQ1	I06 = 1
001	00110	L00EQ1	L00 = 1
001	00111	L0831BEQ0	L08-31 = NONZERO
001	01000	LNEQ0	L00-31 = NONZERO
001	01001	L0709EQ0	L07-09 = 0
001	01010	L1215EQ0	L12-15 = 0
001	01011	XEQFF	X00-07 = ALL ONES
001	01100	C00EQ1	C00 = 1
001	01101	LEXPDF	L01-07 GREATER THAN MANTISSA LENGTH

Table 1-17. Sense and Branch Group 1 (cont)

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
001	01110	ADC001	ADDER CARRY OUT OF BIT 01
001	01111	ONE	1 (+5V.)
001	10000	X0107EQ0	X01-07 = 0
001	10001	ADC008	ADDER CARRY OUT OF BIT 8
001	10010	P38EQ0	PSW38 = 0 UNDERFLOW MASK BIT
001	10011	L0811EQ0	L08=11 = 0
001	10100		
001	10101		
001	10110		
001	10111		

Table 1-18. Sense and Branch Group 2

Current BDW / SAB Field (Bits 1,2,3)	Current Microinstruction / NOTE: Conditions called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
010	00000	BCCOMP	(I01=1 + I12-15 = NONZERO) * CC COMPARE (BC/BCR)
010	00001	RECOMP	(I07=0 * (FF3 NOT EQ. FF4) + I07=1 * (FF3 = FF4)) * FF6 = 0
010	00010	IR2EQ0	I12-15 = 0 (R2 = 0)
010	00011	IR1LT2	I08-10 = 0 (R1 = 0 or 1)
010	00100	FF3NEQFF4	SSF3 NOT EQUAL SSF4
010	00101	IR2EQ1	I12-14 = 0* I15 = 1 (R2 = 1)
010	00110		
010	00111	FF3EQ0	SFF3 -0
010	01000	DNEQ00F1	000-31 = NONZERO + SF1 = 1
010	01001	DNEQD0F1	000-31 = NONZERO + SSF1 = 1
010	01010	BIGOP2	NO ADDER CARRY OUT OF BIT 00 * PSW16-18 = 001
010	01011	ADC000	ADDER CARRY OUT OF BIT 00
010	01100	IPL	INITIAL PROGRAM LOAD
010	01101	FIXDISC	FIXED DISC LOAD DEVICE
010	01110		

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Table 1-18. Sense and Branch Group 2 (cont)

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
010	01111	ZBEQ0	Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 or 010))
010	10000	C2122EQ0	C21-22 = 0
010	10001	C2831EQNEG	(C28-31=B+D)+(C28-31=9) * (P16-18=001) * (FFS+1)
010	10010	ACK	I/O ACKNOWLEDGE
010	10011	IOCCEQ0	I/O CONDITION CODE = 0 (I034-35 = 0)010
010	10100	L31EQ1	L31 = 1
010	10101	I06EQ1	I06 = 1
010	10110	I07	I07 = 1
010	10111	P12EQ1EM	PSW12=1) * (PSW16-18 = 001 or 010)

Table 1-19. Sense and Branch Group 3

Current BDW	Current Microinstruction			
SAB Field (Bits 1,2,3)	NOTE Condition called by SAVE, IF, or BLOCK statements (Restrictions are listed in table 1-25.)			
Group	Code	Mnemonic	Description	
011	00000	I13EQ1	I13 = 1	
011	00001	M31EQ0	MAR31 = 0	
011	00010	I08EQ1	I08 = 1	
011	00011	I14EQ1	I14 = 1	
011	00100	IR1EQIR2	I08-11 = I12-15	(R1 = R2)
011	00101	LEQ0	L00-31 = 0	
011	00110	NRCRS1	I15 = 1 + NOT PDECINTMR	
011	00111	RAT1S1	(I15 = 1 + (T00-23 = NONZERO)) * PDECINTMR	
011	01000	IR1EQ0	I08-11 = 0	(R1 = 0)
011	01001	IR2EQ0	I12-15 = 0	(R2 = 0)
011	01010	XEQ0	X0007 = 0	
011	01011	LNEQ0	L00-31 = NONZERO	
011	01100			
011	01101	Z00E00	Z00 = 0	
011	01110	I06EQ0	I06 = 0	

Table 1-19. Sense and Branch Group 3 (cont)

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
011	01111	IOG07EQ1	I06-07 = 01
011	10000	C1623EQFF	C16-23 = FF (ALL ONES)
011	10001	C2431EQFF	C24-31 = FF (ALL ONES)
011	10010	L00EQ1	L00 = 1
011	10011	LE00AF2	(L00-31 = 0) * SFF2 = 1
011	10100	P3435EQ3	PSW34-35 = 11 (CONDITION CODE)
011	10101	C2629E	C26-29 = 0
011	10110	L2831EQ0	L28-31 = 0
011	10111	L3031EQ0	L30-31 = 0

Table 1-20. Sense and Branch Group 4

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
100	00000	I02EQ1	I02 = 1
100	00001	PMENB0	PMENB0
100	00010	I07EQ1	I07 = 1
100	00011	I03EQ1	I03 = 1
100	00100	PMENB1	PMENB1
100	00101	XEQ0F	X00-07 = 15 (DECIMAL)
100	00110	L00EQ1	L00 = 1
100	00111	L0831NEQ0	L08-31 = NONZERO
100	01000	LNEQ0	L00-31 = NONZERO
100	01001	L1114EQ0	L11-14 = 0
100	01010	L1619EQ0	L16-19 = 0
100	01011	L0007EQ40	L00-07 = 64 (DECIMAL)
100	01100	L01EQ1	L01 = 1
100	01101	L00EQ0	L00 = 0
100	01110	ADC000	ADDER CARRY OUT OF BIT 00

Table 1-20. Sense and Branch Group 4 (cont)

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
100	01111	XEQ01	X00-07 = 1
100	10000	X0107EQ0	X01-07 = 0
100	10001	L0131NEQ0	L01-31 = NONZERO
100	10010	P38EQ1	PSW38 = 1 UNDERFLOW MASK BIT
100	10011	L0811EQ0	L08-11 = 0
100	10100	C00EQ1	C00 = 1
100	10101	X00EQ1	X00 = 1
100	10110	FPDV	L01 = 1 * (FF4 = 0 + (FF3 = 0 * FF6 = 1))
100	10111	FPMY	L01 = 1 * (FF4 = 0 + (FF3 NOT = FF6)) + FF3 = 1 * FF6 = 1

Table 1-21. Sense and Branch Group 5

Current BDW / SAB Field (Bits 1,2,3)	Current Microinstruction / NOTE: Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)			
Group	Code	Mnemonic	Description	
101	00000	IR1EQL0	(I8=0 * I10=0) + (I9=0 * I10=1)	(R1=0-5+A+B)
101	00001			
101	00010	IR2EQ0ZAP	I12-15 = 0 + ((PSW16-18 = 001) * (I05-11 = 0))	
101	00011	IREQHI	I08 = 1 + I09-10 = 11 - I08-11 = 0	(R1 = 6-F, 0)
101	00100	IR1EQ0	I08-11 = 0	(R1 = 0)
101	00101	IR2EQ1	I12-14 = 0 * I15 = 1	(R2 = 1)
101	00110	LO3O7GT9	LO3 = 1 + (L04 = 1 * L05-06 = NONZERO)	(L03-07 > 9)
101	00111	FF3EQ0	SFF3 = 0	
101	01000	XNEQ0	XO0-07 = NONZERO	
101	01001	ACK	I/O ACKNOWLEDGE	
101	01010	FF1EQ0	SFF1 = 0	
101	01011	ADC000	ADDER CARRY OUT OF BIT 00	
101	01100			
101	01101			

REVISION: HCB-2
COMPANY CONFIDENTIAL

Table 1-21. Sense and Branch Group 5 (cont)

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
101	01110		
101	01111	ZBEQ0	Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 or 010))
101	10000	C2431NEQ00F5	C24-31 = NONZERO + SFF5 = 1
101	10001	C2831EQNEG	(C28-31 = B + D) + (C28-31 = 9)*(P16-18 = 001)*(FF5 = 1)
101	10010	ONE	1 (+5V.)
101	10011	ADC028	ADDER CARRY OUT OF BIT 28
101	10100	L31EQ1	L31 = 1
101	10101	FF35GEQ100	(FF3=1) * (FF5=0) * (FF6=0)
101	10110	FF3EQFF4	SFF3 = SFF4
101	10111	P12EQ1EM	(PSW12 = 1) * (PSW16-18 = 001 or 010)

Table 1-22. Sense and Branch Group 6

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Condition called by SAFE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
110	00000	C2427EQNUM	C24-27 = 1-9
110	00001	C2831EQDIG	C28-31 = 0-9
110	00010	IR1EQ0	I08-11 = 0 (R1 = 0)
110	00011	IREQ0	I08-15 = 0 (R = 0)
110	00100	C2831EQMIN	C28-31 = B + C28=31 = D
110	00101	IR2EQ0	I12-15 = 0
110	00110	L31EQ1	L31 = 1
110	00111	P1618EQ1OR2	PSW16-18 = 001 or 010
110	01000	FF6EQ1	SFF6 = 1
110	01001	FF3EQ0	SFF3 = 0
110	01010	FF4EQ0	SSF4 = 0
110	01011	P12EQ1	PSW12 = 1
110	01100	ZTEST	((Z00-07 NOT 0) * (SFF4=0) + (Z08-15 NOT 0)*(SFF4=1))*I07=1
110	01101	I07EQ1	I07 = 1

REVISION: HCB-2
COMPANY CONFIDENTIAL

Table 1-22. Sense and Branch Group 6 (cont)

Current BDW	Current Microinstruction		
SAB Field (Bits 1,2,3)	NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
110	01110	X07EQ1	X07 = 1
110	01111	ZBEQ0	Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 or 010)
110	10000	ONE	1 (+5V.)
110	10001	NSRFF	SYSTEM RESET FLIP-FLOP = 0
110	10010	OVFLCVB	FF = 1 + L00 = 1 * (FF4=0 + 101-31≠0)
110	10011	ZPAT1	Z BYTE (SFF1) = DIGIT SELECT OR SIGNIFICANCE START
110	10100	IR1EQ0D2	I08-11 = 0 + SFF5 = 1
110	10101		
110	10110		
110	10111		

Table 1-23. Sense and Branch Group 7

Current BDW	Current Microinstruction			
SAB Field (Bits 1,2,3)	NOTE Condition called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)			
Group	Code	Mnemonic	Description	
111	00000	FF3NEQFF4	SFF3 NOT EQUAL SFF4	
111	00001	IREQ1	I08-14 = 0 * I15 = 1	(R = 1)
111	00010	XEQ0	X00-07 = 0	
111	00011	FF234EQ101	(SSF2 = 1) * (SFF3 = 0) * (SFF4 = 1)	
111	00100	IRNEQ00F5	(I08-15 = NONZERO) + (SFF5 = 1)	
111	00101	IREQ0	I08-15 = 0	(R = 0)
111	00110	M31EQ1	MAR31 = 1	
111	00111	ONE	1 (+5V.)	
111	01000	OP1LW	(I08-15 = 0) + ((I08-15 = 1) * (SFF5 = 0))	
111	01001	FF3EQ0	SFF3 = 0	
111	01010	FF4EQ0	SFF4 = 0	
111	01011	I06EQ1	I06 = 1	
111	01100	IREQONF25	(I08-15 = 0) * (SFF2 = 0) * (SFF5 = 0)	
111	01101	I05EQ0	I05 = 0	
111	01110	ADC000	ADDER CARRY OUT OF BIT 00	

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Table 1-23. Sense and Branch Group 7 (cont)

Current BDW / SAB Field (Bits 1,2,3)	Current Microinstruction NOTE Conditions are called by SAVE, IF, or BLOCK statements. (Restrictions are listed in table 1-25.)		
Group	Code	Mnemonic	Description
111	01111	ZBEQ0	Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 or 010))
111	10000	L2431NEQ0	L24-31 = NONZERO
111	10001	L1631NEQ0	L16-31 = NONZERO
111	10010	BYTEM	(L08-31 = 0)
111	10011	CNEQ0	C00-31 = NONZERO
111	10100	C00EQ1	C00 = 1
111	10101	D0001NEQ0	D00-01 = NONZERO
111	10110	D0002NEQ0	D00-02 = NONZERO
111	10111	X0005EQ0	X00-05 = 0

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Table 1-24. Sense and Branch Group 8

NOTE

Group 8 available only as second sense condition (C2) in statement: SAVE C1·C2 IN FF1,2 (irregardless of BDW in SAB field). The 3 least significant bits of C2 must be the same code as C1.

Group	Code	Mnemonic	Description
SC2	XX000	OVFL	D DIGITS SELECTED BY (I09-12) = NONZERO
SC2	XX001	OVFL2	D00-31 = NONZERO + SFF2 = 1
SC2	XX010	FF2EQ0	SFF2 = 0
SC2	XX011	ZPAT2	Z BYTE (SFF1) = DIGIT SELECT OR FIELD SEPARATOR
SC2	XX100	IR1EQ001	I08-11 = 0 + (SFF5 = 0) * (I12-15 = NONZERO)
SC2	XX101	C3031EQ0	C30-31 = 0
SC2	XX110	L0107NEQ0	L01-07 = NONZERO
SC2	XX111	X0607EQ3	X06-07 = 11

REVISION: HCB-2

COMPANY CONFIDENTIAL

MH2438

Table 1-25. Program Exception Equations

PX GROUP	INT CODE	MNEMONIC	DESCRIPTION
000	000	MSTORE	Main Store Errors
000	001	DWB	
000	010	FWB	
000	011	HWB	
000	100	R1ODD	
000	101	IMOREE	
000	110	FXOVF	
000	111	FXDIV	
001	000	MSTORE	
001	001	DWB	
001	010	FWB	
001	011	SIGNIF	
001	100	R12ODD	
001	101	EXPUNF	
001	110	EXPOVF	
001	111	FLDIV	
010	000	MSTORE	
010	001	DWB	
010	010	QWB	
010	011	DIGIT	
010	100	SIGN	
010	101	IOSTSRER	
010	110	CSW ADR	
010	111	FXD1V	
011	000	MSTORE	
011	001	L2GT7	
011	010	L1LEL2	
011	011	DIGIT	
011	100	SIGN	
011	101	LZEROS	
011	110	DECOVF	
011	111	DECDIV	

NOTE: Bit Ø of the BDW PX field is not implemented; only 4 PX groups are available.

Table 1-26. SAVE, IF, BLOCK Restrictions For Sense and Branch Conditions

Statement	Restrictions
SAVE C1 IN FFn (n=1-6) SAVE C1,C2 IN FF1,2	The condition specified as C1 may be any one of the specific group (0-7) selected by the SAB field of the current BDW; the condition specified as C2 must be the specific one from group 8 whose SNSC code has the same low-order 3 bits as does the code for C1.
IF C1, C2 GOTO	The condition specified as C1 may be F, T, FF1, FF3, FF5, or a sense condition having code 0, 1, 2 in the group selected by the SAB field of the current BDW; the condition specified as C2 may be F, T, FF2, FF4, FF6, or a sense condition having code 3, 4, or 5 in the group selected by the SAB field of the current BDW.
BLOCK MSTORE IF C1	This condition specified as C1 may be any one of the specific group (0-7) selected by the SAB field of the current BDW.

Table 1-27. Microinstruction Field Definitions

Field	Bits	Mnemonic	Function
			Select A input to shifter
	000	Ø	Zeros → SA0-31
	001	Z	Z0-15 → SA0-15; Z0-15 → SA16-31
	010	L	L0-31 → SA0-31
SA	011	C	C0-31 → SA0-31
(3 bits)	100	MAINT	MAINT 0-15 → SA0-15; MAINT 0-15 → SA16-31
	101	LR16	L0-15 → SA16-31; Zeros → SA0-15
	110	-	Undefined
	111	-	Undefined
			Select B input to shifter
	000	Ø	Zeros → SB0-31
	001	Z0-15	Z0-15 → SB0-15; Z0-15 → SB16-31
	010	L	L0-31 → SB0-31
SB	011	C	C0-31 → SB0-31
(3 bits)	100	MAINT	MAINT 0-15 → SB0-15; MAINT 0-15 → SB16-31
	101	CR16	C0-15 → SB16-31; Zeros → SB0-15
	110	KIGR	Key IGR0-3 → SB25-28; Zeros → SB0-24, 29-31
	111	HINT	Interrupt Code 0-7 → SB24-31; Zeros → SB0-23

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
			Shift control Where OV is not mentioned, it is not changed. Otherwise, all unspecified bits of S and OV are zero filled. A and B refer to any group 1 and group 2 destinations, respectively.
S (5 bits)	00 000	-	SA0-31 → S0-31; SB0-31 → S32-63
	00 001	A,R1	SA0-30 → S1-31; SB0-31 → S32-63
	00 010	A,R2	SA0-29 → S2-31; SB0-31 → S32-63
	00 011	A,R4	SA0-27 → S4-31; SB0-31 → S32-63; SA28-31 → OVØ-3
	00 100	A,R8	SA0-23 → S8-31; SB0-31 → S32-63; SA24-31 → OVØ-7
	00 101	A,L1	SA1-31 → S0-30; SB0-31 → S32-63
	00 110	A,L2	SA2-31 → S0-29; SB0-31 → S32-63
	00 111	A,L4	SA4-31 → S0-27; SB0-31 → S32-63; SA0-3 → OV4-7
	01 000	-	SA0-31 → S0-31; SB0-31 → S32-63
	01 001	AB,R1	SA0-31 → S1-32; SB0-30 → S33-63
	01 010	AB,R2	SA0-31 → S2-33; SB0-29 → S34-63; B3Ø,31 → OVØ,1
	01 011	AB,R4	SA0-31 → S4-35; SB0-27 → S36-63
	01 100	AB,R8	SA0-31 → S8-39; SB0-23 → S40-63
	01 101	AB,L1	SA1-31 → S0-30; SB0-31 → S31-62
	01 110	AB,L2	SA2-31 → S0-29; SB0-31 → S30-61
	01 111	AB,L4	SA4-31 → S0-27; SB0-31 → S28-59
	10 000	B,R1A	SA0-31 → S0-31; SB0 → S32; SB0-30 → S33-63; SB31 → OVØ
	10 001	B,R1C	SA0-31 → S0-31;OVB0 → S32; SB0-30 → S33-63; SB31 → OVØ
	10 010	B,R4A	SA0-31 → S0-31; SB0 → S32-35; SB0-27 → S36-63, SB28-31 → OVØ-3
	10 011	B,R4C	SA0-31 → S0-31;OVB0-3 → S32-35; SB0-27 → S36-63; SB28-31 → OVØ-3
	10 100	B,R8C	SA0-31 → S0-31;OVB0-7 → S32-39; SB0-23 → S40-63;SB24-31 → OVØ-7
	10 101	B,L1C	SA0-31 → S0-31;OVB7 → S63; SB1-31 → S32-62; SB0 → OV7
	10 110	-	Undefined
	10 111	B,L4C	SA0-31 → S0-31;OVB4-7 → S60-63; SB4-31 → S32-59; SB0-3 → OV4-7.

REVISION: HCB-2

COMPANY CONFIDENTIAL

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
			Shift control (cont)
S (5 bits) (cont)	11 000	-	SA0-31 → S0-31; SB0-31 → S32-63
	11 001	B,R1	SA0-31 → S0-31; SB0-30 → S33-63; SB31 → OVØ
	11 010	B,R2	SA0-31 → S0-31; SB0-29 → S34-63
	11 011	B,R4	SA0-31 → S0-31; SB0-27 → S36-63; SB28-31 → OVØ-3
	11 100	B,R8	SA0-31 → S0-31; SB0-23 → S40-63
	11 101	B,L1	SA0-31 → S0-31; SB1-31 → S32-62; SB0 → OV7
	11 110	B,L2	SA0-31 → S0-31; SB2-31 → S32-61
	11 111	B,L4	SA0-31 → S0-31; SB4-31 → S32-59; SB0-3 → OV4-7
			IGR A Address
AAD (4 bits)	0000	AØ	Location 0 Instruction Halfword
	0001	A1	Location 1 First Operand Address
	0010	A2	Location 2 Operand Address
	0011	A3	Location 3 Working Register
	'	'	'
	'	'	'
	1101	AD	Location D Working Register
	1110	AE	Location E Working Register
	1111	AF	Location F Working Register

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
AWE (3 bits)			IGR A Write Enable Unspecified bits of IGR A are not changed.
	000	-	Do not write to IGR A
	001	An,HI	S0-15 → An0-15 High halfword (Bytes Ø and 1)
	010	An,LO	S16-31 → An16-31 Low halfword (Bytes 2 and 3)
	011	An,FW	S0-31 → An0-31 Fullword
	100	An,SBØ	S0-7 → An0-7 Byte Ø
	101	An,SB1	S8-15 → An8-15 Byte 1
	110	An,SB2	S16-23 → An16-23 Byte 2
	111	An,SB3	S24-31 → An24-31 Byte 3
BAD (4 bits)			IGR B Read Address
	0000	B1	General Register 1
	0001	B2	General Register 2
	0010	BR1	*General Register specified by R1 field of I register
	0011	BR2	*General Register specified by R2 field of I register
	0100	BX	General Register specified by X 0-3
	0101	BR1N	*General Register specified by R1+1 if R1 is even
	0110	BR2N	*General Register specified by R2+1 if R2 is even
	0111	-	Undefined
			*When the Working IGR B flip-flop is set, microorders BR1, BR2, BR1N, BR2N address the working or floating-point registers rather than the general registers.

REVISION: HCB-2

COMPANY CONFIDENTIAL

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
BAD (4 bits) (cont)			IGR B Read Address (cont)
	1000	B28	Location 28 Instruction Address
	1001	B29	Location 29 Relocation Offset
	1010	B2A	Location 2A Working Register
	1011	B2B	Location 2B Working Register
	1100	B2C	Location 2C Working Register
	1101	B2D	Location 2D Working Register
	1110	B2E	Location 2E Working Register
	1111	B2F	Location 2F Working Register
BWAD (4 bits)			IGR B Write Address This field is interpreted in the same way as the BAD field. If the BWAD field is missing (Hfield ≠ 00), the write address is the same as the read address (BAD).
BWE (4 bits)			IGR B Write Enable
	0000	-	Do not write to IGR B
	lxxx	*BRn,SBØ	S32-39 → BRn 0-7 Byte 0
	xlxx	*BRn,SB1	S40-47 → BRn 8-15 Byte 1
	xxlx	*BRn,SB2	S48-55 → BRn 16-23 Byte 2
	xxxl	*BRn,SB3	S56-63 → BRn 24-31 Byte 3
	1111	*BRn,FW	S32-63 → BRn 0-31 Full Word
			Unspecified bits of IGR B are not changed.
			*BRn = BR1, BR2, BR1N, BR2N, BX, B1, B2, B28-2F.

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
			Format Control
H (2 bits)	00		Enable BWAD decode; disable W and SM decodes
	01		Enable W and SM decodes; disable BWAD decodes
	10		Undefined
	11		Load BDW (Branch Discipline Word) disable SB, S, BWE, BWAD, W, SM, M, SC, F, CAR, INT, SNSC, SNSF
			Load WDR
W (2 bits)	00	-	Do not change WDR
	01	WDR,SB1	S48-55 ⟶ WDR8-15 Byte 1 crossover (B2 ⟶ B1)
	10	WDR,SBØ	S56-63 ⟶ WDRØ-7 Byte Ø crossover (B3 ⟶ BØ)
	11	WDR,HW	S48-63 ⟶ WDRØ-15 Half Word
			Unspecified bits of WDR are not changed.
			Select Input to MAR
SM (2 bits)	00	-	Do not change MAR
	01	BRn	B8-31 ⟶ MAR 8-31
	10	An	A8-31 ⟶ MAR 8-31 } MAR Ø-7 does not exist
	11	L	ADDER 8-31 ⟶ MAR 8-31

REVISION: HCB-2

COMPANY CONFIDENTIAL

#RH2438

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
			Select Input to C Register
	000	-	Do not change C
	001	BRn	B0-31 → C0-31
	010	An	A0-31 → C0-31
SC	011	PSWH	PSW0-31 → C0-31
(3 bits)	100	PSWL	PSW32-39 → C0-7; B8-31 → C8-31; Address IGR B28
	101	Ø	Zeros → C0-31
	110	X	X0-7 → C0-7; Zeros → C8-31
	111	IOST SOFT	IOST5-15 → C5-15; SOFTSCOPE 0-7 → C16-23; SFF1-6 → C24-29; Zeros → C0-4, 30-31
			Select First Operand to Adder
	000	Ø	Zeros → DA 0-31
	001	An	A 0-31 → DA 0-31
	010	Z	**Z4-15 → DA 20-31; Zeros → DA 0-19
DA	011	C	C 0-31 → DA 0-31
(3 bits)	100	OVL	OV 0-7 → DA 24-31; Zeros → DA 0-23
	101	OVH	OV 0-7 → DA 0-7; Zeros → DA 8-31
	110	Enn	*K 0-31 → DA 0-31
	111	RBn	B 0-31 → DA 0-31

*As defined by E and ED fields.

**Modified by PSW mode controls as follows if Z0=0:
Z 2-15 → DA 18-31; Zeros → DA 0-17 for 360/20 mode.
Z 1-15 → DA 17-31; Zeros → DA 0-16 for 9200/9300 mode.

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
DB (3 bits)			Select Second Operand to Adder
	000	-	Zeros → DB 0-31
	001	BRn	B 0-31 → DB 0-31
	010	-	TIMER 0-23 → DB 8-31; Zeros → DB 0-7
	011	An	A 0-31 → DB 0-31
	100	OVL	OV 0-7 → DB 24-31; Zeros → DB 0-23
	101	OVH	OV 0-7 → DB 0-7; Zeros → DB 8-31
	110	Enn	*K 0-31 → DB 0-31
	111	TWO	one → DB 30; Zeros → DB 0-29, 31
			*As defined by E and ED fields.
F (3 bits)			Adder Function
	000	ADD	Binary Add
	001	SUB	Binary Subtract (add ones complement of DB)
	010	AND	Logical AND
	011	OR	Inclusive OR
	100	XOR	Exclusive OR
	101	OPC	Function specified by BDW AF field
	110	-	Undefined
	111	-	Undefined
			The decimal subtract function specified by BDW effectively adds the nines complement of DB to DA.
			The digit carries are automatically saved for decimal correction.
			Latch and carry-out are strobed at clock 2.
			Carry-in must be specified in CAR field.

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Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
			Carry Into Adder
CAR (2 bits)	00	CØ	Add zero to bit 31
	01	C1	Add one to bit 31
	10	CP	Add to bit 31 the previous carry-out from bit Ø
	11	CS	Add to bit 31 the current content of Sense flip-flop 5
			Carry-out is loaded at clock 2, buffer at clock 4.
			Main Store Controls
M (3 bits)	000	-	Do not initiate main store
	001	-	Do not initiate main store
	010	-	Do not initiate main store
	011	-	Do not initiate main store
	100	READ	Initiate read halfword
	101	WRITE,SB1	Initiate write byte 1
	110	WRITE,SBØ	Initiate write byte 0
	111	WRITE	Initiate write halfword
			Note that the most significant bit of the M field controls main store initiation.

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
INT (3 bits)			Program Exception Interrupt Controls The interpretation of this field depends on the value of the PX field of the current BDW, as summarized below. Note that bit Ø of the PX field is not implemented. Main Store Data error checked at clock 3. Other Main Store errors checked at clock 2. All other errors checked at clock 4.

	BDW PX = 000	BDW PX = 001	BDW PX = 010	BDW PX = 011
000	Main Store	Main Store	Main Store	Main Store
001	D.W. Boundary	D.W. Boundary	D.W. Boundary	L2 > 7
010	F.W. Boundary	F.W. Boundary	Q.W. Boundary	L1 ≤ L2
011	H.W. Boundary	Significance	Invalid Digit	Invalid Digit
100	R1 Odd	R1 or R2 Odd	Invalid Sign	Invalid Sign
101	STR Modifier	Exp. Underflow	IOST Stge.Er.	Leading Zeros
110	Fx.Pt.Overflow	Exp. Overflow	--	Dec. Overflow
111	Fx.Pt.Divide	Flt.Pt.Divide	Fx.Pt.Divide	Dec. Divide

Field	Bits	Mnemonic	Function
SNSC (5 bits)			Sense condition source The SNSC field selects the sense conditions to be saved in the sense flip-flops selected by the SNSF field. Under control of SAB field of BDW (See tables 1-15 thru 1-23.)

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
SNSF (3 bits)			Sense destination flip-flop
	000	-	Do not change any sense flip-flops
	001	FF1	Load flip-flop 1 with SNSC condition
	010	FF2	Load flip-flop 2 with SNSC condition
	011	FF3	Load flip-flop 3 with SNSC condition
	100	FF4	Load flip-flop 4 with SNSC condition
	101	FF5	Load flip-flop 5 with SNSC condition
	110	FF6	Load flip-flop 6 with SNSC condition (not dbl. gated)
	111	FF1,2	Load flip-flop 1 and 2 with SNSC conditions
			Sense flip-flop 6 is a set-reset flip-flop which can only be set by this field. The others are jam-set (double-gated) flip-flops which can be set or cleared.
E (8 bits)			Emit constant
			This field contains an 8-bit literal constant E, which is available as an adder operand if the JC field is 010, 011, 100, 110.
ED (3 bits)			Emit destination
	000	Enn,SB3	E0-7 → K24-31; Zeros → K0-23
	001	Enn,SBØ	E0-7 → K0-7; Zeros → K8-31
	010	Enn,FW	E0-7 → K0-7, 8-15, 16-23, 24-31
	011	Enn,LS2	E0-7 → K22-29; Zeros → K0-21, 30-31
	100	-	Undefined
	101	BDW,Enn	E0-7 → BDW (E0-2 → SAB1-3,E3 not used, E4-5 → PX1-2,E6-7 → MSC0-1)
	110	CC,Enn	E6-7 → PSW34-35 (Condition Code)
	111	-	Undefined
			K is not a register, but merely serves to define the 32-bit constant called for by DA=110 or DB=110.

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
			Mark control
MK (1 bit)	0		Do not change MARK register
	1		MARK Load MARK with address of current microinstruction + 1.
			MARK register is automatically loaded with PTR field (11 bits) whenever BDW is loaded.
			Jump control
JC (3 bits)	000	GOTO	Unconditionally go to address in E and ED
	001	IF	Conditional branch (concatenate)
	010	MARK	*Jump to address in MARK register
	011	default	*Go to next address in sequence (+1)
	100	OPC	*Jump to OP CODE
	101	OPEn	Jump to OP CODE and EO-2 (E≠Ø)
	110	-	*Undefined
	111	IF.BDW	Conditional branch with most significant address bits = 0010
			*E field is available for generating constants.
			See table 1-27 for JC Field definitions.
		Clock	
MISC (6 bits) Group Ø	000000	-	Null
	000001	2	Move Ø → KEY register
	000010		Stop if Instruction Mode
	000011		Set Stat. (Start Staticizing), Clears BDW register at clock 2 and starts error logic path.
	000100		Stop (HPR)
	000101	4	Block Write to IGR B if IO-1=00; step ILC + 1 if IO-1≠00; Load X (SO-7 → XO-7).

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic Clock	Function
MISC (6 bits)	000110		Block Main Storage Initiate if Z0-1=00; Set ILC=1; Load I(S16-31 → I00-15). Set Condition Code according to BDW CC
(cont)	000111		Set CC (Set Condition Code according to BDW CC).
Group Ø			
BDW MSC = ØØ	001000	3	Move S16-31 → I0-15 (OP,R1,R2)
	001001	3	Move S0-7 → X0-7
	001010	3	Step X+1
	001011	3	Step X-1
	001100	4	Step ILC+1
	001101	4	Set ILC=1
	001110	4	Clear ILC
	001111		-
	010000	2	Move PSW 9-11 → KEY register
	010001	4	Move S32-63 → PSW 0-31 (PSWH)
	010010	4	Move S56-63 → PSW24-31 (PSWH, SB3)
	010011	4	Move S34-39 → PSW34-39 (PSWL)
	010100		Set Vulnerable Main Storage Reference
	010101		Set Hardware Main Storage Reference
	010110		-
	010111	2	Clear SFF 1-6

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Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
		Clock	
MISC (6 bits) Group Ø BDW MSC = ØØ	011000	1	Set Hardware Masks: PX on clock 1, MC on Clock 2
	011001	1,2	Clear Hardware Masks
	011010		-
	011011		-
	011100	1	Clear IOST $SSRA_x$ flip-flop
	011101	1	Clear IRF being serviced
	011110	2	Set SVC Interrupt
	011111	1	Set Inhibit Interrupt if I 15=1
			Unspecified entries are undefined and perform no function.
MISC (6 bits) Group 1 BDW MSC = Ø1	000000	-	Null
	000001	2	Move Ø ⟶ KEY register
	000010		Stop if Instruction Mode
	000011		Set Stat. (Start Staticizing)
	000100		Stop (HPR)
	000101		-
	000110		-
	000111		Set Condition Code according to BDW CC
	001000	3	Move S24-31 ⟶ I 8-15 (R1, R2)
	001001	3	Move S0-7 ⟶ X 0-7
	001010	3	Step X+1
	001011	3	Step X-1

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic Clock	Function
MISC (6 bits) (cont)	001100	4	Step ILC+1
	001101		-
	001110		-
	001111		-
Group 1 BDW MSC = Ø1	010000	2	Move PSW 9-11 → KEY register
	010001	2	Move C5-7 → KEY register
	010010		-
	010011		-
	010100		Set Vulnerable Main Storage Reference
	010101		Set Hardware Main Storage Reference
	010110		-
	010111	2	Clear SFF1-6
	011000		-
	011001		-
	011010		-
	011011		-
	011100	1	Clear IOST $SRRA_x$ flip-flop
	011101	1	Clear IRF being serviced; set IOST IRF (Interrupt Request)
	011110	4	Set IOST STF (Status Table Full)
	011111	1	Set IOST Suspend State
			Unspecified entries are undefined and perform no function.

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
		Clock	
	000000	-	Null
	000001	2	Move Ø ⟶ KEY register
MISC	000010		Stop if Instruction Mode
(6 bits)	000011		Set Stat. (Start Staticizing)
	000100		Stop (HPR)
Group	000101		Block Half Adder for one cycle unconditionally
2	000110		-
	000111		Set Condition Code according to BDW CC
BDW MSC			
= 10	001000	3	Move S24-31 ⟶ I 8-15 (R1, R2)
	001001	3	Move S 0-7 ⟶ X 0-7
	001010	3	Step X+1
	001011	3	Step X-1
	001100	4	Step ILC+1
	001101		-
	001110		-
	001111		-

REVISION: HCB-2

COMPANY CONFIDENTIAL

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
		Clock	
	010000	2	Move PSW 9-11 → KEY register
	010001		-
MISC	010010	4	Move S32-39 → PSW 0-7 (PSWH, SB0)
(6 bits)	010011	4	Move S34-39 → PSW34-39 (PSWL)
(cont)	010100		-
	010101		-
Group	010110		Set Sync. Check (Softscope); Inhibit Stall Timer
2	010111	2	Clear SFF1-6
	011000	3	Set SIO
BDW MSC	011001	3	Clear SIO
= 10	011010	4	Read Key IGR Buffer to SB selector
	011011	3	Move C25-28 → KEY IGR
	011100	1	Clear TIMER-ON FF
	011101	1	Set TIMER-ON FF if I 15 = 0
	011110	1	Clear TIMER Interrupt Request if I 13 = 1 or I 15 = 1
	011111	1	Move B8-31 → TIMER 0-23
			Unspecified entries are undefined and perform no function.

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
		Clock	
	000000	-	Null
	000001	2	Move Ø ⟶ KEY register
	000010		Stop if Instruction Mode
	000011		Set Stat. (Start Staticizing)
MISC (6 bits)	000100		Stop (HPR)
	000101		Step IR1+1 and IR2-2
Group 3	000110		Block Main Storage Initiate if SNSC is true
	000111		Set Condition Code according to BDW CC
BDW MSC = 11	001000	3	Move S24-31 ⟶ I 8-15 R1, R2)
	001001	3	Move S0-7 ⟶ X0-7
	001010	3	Step X+1
	001011	3	Step X-1
	001100	4	Step ILC+1
	001101	4	Set Working IGR B access flip-flop
	001110	4	Set Problem IGR B access (one cycle only)
	001111	3	Set Decode of C30, C31

Table 1-27. Microinstruction Feild Definitions (cont)

Field	Bits	Mnemonic	Function
		Clock	
MISC (6 bits) (cont) Group 3 BDW MSC = 11	010000	2	Move PSW 9-11 → KEY register
	010001	2	Clear SFF1
	010010	2	Clear SSF2
	010011	2	Clear SFF3
	010100	2	Clear SFF4
	010101	2	Clear SFF5
	010110	2	Clear SSF6
	010111	2	Clear SFF1-6
	011000		Step IR1-1 and IR2-2
	011001		Step IR1+1
	011010		Step IR1-1
	011011		Step IR1-2
	011100		Step IR2-1
	011101		Step IR2-2
	011110		Step IR-1
	011111		Step IR-2
			Unspecified entries are undefined and perform no function.

Table 1-27. Microinstruction Field Definitions (cont)

Field	Bits	Mnemonic	Function
		Clock	
MISC FUNCT. AVAIL. ALL GROUPS	100000		Set working IGR B access flip-flop; stop if Instruction Mode
	100001		Set LDCS flip-flop (Load Control Store)
	100010		Set WTIR flip-flop (Wait for Status Table Interrupt Request)
	100011		Set TREAD flip-flop (Control Store Test Read)
	100100		Clear ROM flip-flop (Read-Only Memory access)
	100101		Set ROM flip-flop (Read-Only Memory access)
	100110		Set Write to Control Store, using address in C register
	100111		Clear Control Store address counters
	101000		Set Processor Check and HPR Stop
	101001		Clear Working IGR B access flip-flop
	101010		Step IR1+1 and IR2-1
	101011		Step IR1-1 and IR2-1
	101100		Set System Reset
	101101		-
	101110		-
	101111		-

Table 1-28. Branch Address Formation-JC Field Addresses

JC Field	Address Bits										
	Ø	1	2	3	4	5	6	7	8	9	10
Ø	E Ø	E 1	E 2	E 3	E 4	E 5	E 6	E 7	ED Ø	ED 1	ED 2
1	ACT Ø	ACT 1	ACT 2	ACT 3	E Ø	E 1	E 2	E 3	E 4	CATSEL Ø	CATSEL 1
2	MK Ø	MK 1	MK 2	MK 3	MK 4	MK 5	MK 6	MK 7	MK 8	MK 9	MK 1Ø
3	ACT Ø	ACT 1	ACT 2	ACT 3	ACT 4	ACT 5	ACT 6	ACT 7	ACT 8	ACT 9	ACT 1Ø
4	Ø	Ø	Ø	I Ø	I 1	I 2	I 3	I 4	I 5	I 6	I'7
5	E Ø	E 1	E 2	I Ø	I 1	I 2	I 3	I 4	I 5	I 6	I 7
6	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
7	Ø	Ø	1	Ø	E Ø	E 1	E 2	E 3	E 4	CATSEL Ø	CATSEL 1

E5-7	CATSEL Ø
Ø	Ø
1	Sense FF1
2	Sense FF3
3	Sense FF5
4	Sense Data Ø
5	Sense Data 1
6	Sense Data 2
7	1

ED0-2	CATSEL 1
Ø	Ø
1	Sense FF2
2	Sense FF4
3	Sense FF6
4	Sense Data 3
5	Sense Data 4
6	Sense Data 5
7	1

Table 1-29. Condition Code Equations

BDW CC GROUP	STATIC DECODE FOR PSW34	STATIC DECODE FOR PSW35
00000	do not change CC	do not change CC
00001	SFF1	SFF2
00010	I034 (I/O CC bit Ø)	I035 (I/O CC bit 1)
00011	SSF1*SFF6	SFF1*SFF6
00100	Ø	SFF6
00101	SFF1*SFF5*SFF6 + SFF1*SFF5*SFF6	SFF1*SFF5*SFF6 + SFF1*SFF5*SFF6
00110	1 (unused)	1 (unused)
00111	1 (unused)	1 (unused)
01000	1 (unused)	1 (unused)
01001	1 (unused)	1 (unused)
01010	1 (unused)	1 (unused)
01011	1 (unused)	1 (unused)
01100	1 (unused)	1 (unused)
01101	1 (unused)	1 (unused)
01110	1 (unused)	1 (unused)
01111	1 (unused)	1 (unused)
10000	SW34 + OVERFLOW + NOSHIFT* LOO* (LOO-31=0 + SFF6)	PSW35 + OVERFLOW + NOSHIFT*LOO
10001	CORO (carry out of bit Ø)	LOO-31=0
10010	Ø	LOO-31=0
10011	(LOO*LOO-31=0 + UFOVF1)*IOO*NATIVEMD + L16*L16-31=0*(IOO + 36020MD + 929300MD) + UFOVF2*(IOO*IO1*IO2*IO3 + 929300MD)	(LOO+UFOVF1)*IOO*NATIVEMD + L16*(IOO + 36020MD + 929300MD) + UFOVF2*(IOO*IO1*IO2*IO3 + 929300MD)
10100	LOO*LOO-31=0	LOO
10101	CORO*LOO-31=0*IOO + COR24*L24-31=0*IOO	CORO*IOO + COR24*IOO
10110	NATIVEMD*LOO-31=0*(XORO*CORO + XORO*CORO) + NATIVEMD*LOO-31=0*(XOR16*COR16 + XOR16*COR16)	NATIVEMD*(XORO*CORO + XORO*CORO) + NATIVEMD*(XOR16*COR16 + XOR16*COR16)

REVISION: HCB-2

COMPANY CONFIDENTIAL

Table 1-29. Condition Code Equations (cont)

BDW CC GROUP	STATIC DECODE FOR PSW34	STATIC DECODE FOR PSW35
10111	1 (unused)	1 (unused)
11000	$\overline{SFF4}$*SFF6	SFF4*SFF6
11001	SFF1*(X0-7=0)	$\overline{X0-7=0}$
11010	$\overline{SFF3}$*SFF6 + SFF5	SFF3*SFF6 + SFF5
11011	SFF1*$\overline{SFF3}$*SFF4 + $\overline{SFF3}$*SFF4*$\overline{SFF5}$ + SFF1*SFF3*SFF4*SFF6 + SFF1*SFF3*$\overline{SFF4}$*SFF6	SFF1*SFF3*$\overline{SFF4}$ + SFF3*$\overline{SFF4}$*$\overline{SFF5}$ + SFF1*SFF3*SFF4*SFF6 + SFF1*$\overline{SFF3}$*$\overline{SFF4}$*$\overline{SFF6}$
11100	SFF1*SFF3 + SFF2 + SFF3*SFF4*$\overline{SFF5}$*SFF6 + $\overline{SFF3}$*SFF4*$\overline{SFF5}$*SFF6	SFF1*SFF3 + SFF2 + SFF3*SFF4*$\overline{SFF5}$*SFF6 + $\overline{SFF3}$*$\overline{SFF4}$*SFF5*SFF6
11101	SFF1*$\overline{SFF3}$ SFF2 + SFF3*$\overline{SFF4}$*$\overline{SFF5}$*SFF6 + $\overline{SFF3}$*SFF4*$\overline{SFF5}$*SFF6	SFF1*SFF3 + SFF2 + SFF3*$\overline{SFF4}$*$\overline{SFF5}$*SFF6 + $\overline{SFF3}$*SFF4*$\overline{SFF5}$*SFF6
11110	1 (unused)	1 (unused)
11111	1 (unused)	1 (unused)

NOTES FOR TABLE 1-29. Condition Code Equations

In the following equations, S refers to the S field of the microinstruction.

OVERFLOW = (S=1X101)*(C00*$\overline{C01}$ + $\overline{C00}$*C01) + (S=1x111)*($\overline{C00}$*(C01+C02+C03+C04) + C00*($\overline{C01}$+$\overline{C02}$+$\overline{C03}$+$\overline{C04}$)

NOSHIFT = (S=00000)

UFOVF1 = COR00*$\overline{COUT01}$ + $\overline{COR00}$*COUT01

UFOVF2 = COR16*$\overline{COUT17}$ + $\overline{COR16}$*COUT17

NATIVEMD = PSW16-18 = 000

929300MD = PSW16-18 = 001

36020MD = PSW16-18 = 010

COR = Carry Out Register

COUT = Carry Out from Adder

XOR = Exclusive OR of Adder input operands

\+ = Logical OR

* = Logical AND

REVISION: HCB-2

COMPANY CONFIDENTIAL

Table 1-30. Sense Information Listed By Register

Register Description	Grp	Code	Mnemonic
1 (+5 V,)	000	01101	ONE
1 (+5 V,)	001	01111	ONE
1 (+5 V,)	101	10010	ONE
1 (+5 V,)	110	10000	ONE
1 (+5 V,)	111	00111	ONE
ADDER CARRY OUT OF BIT 00	010	01011	ADC000
NO ADDER CARRY OUT OF BIT 00 * PSW16-18 = 001	010	01010	BIGOP2
ADDER CARRY OUT FO BIT 00	100	01110	ADC000
ADDER CARRY OUT OF BIT 00	101	01011	ADC000
ADDER CARRY OUT OF BIT 00	111	01110	ADC000
ADDER CARRY OUT OF BIT 01	001	01110	ADC001
ADDER CARRY OUT OF BIT 08	001	10001	ADC008
ADDER CARRY OUT OF BIT 26	101	10011	ADC028
C00 = 1	001	01100	C00EQ1
C00 = 1	100	10100	C00EQ1
C00 = 1	111	10100	C00EQ1
C00-31 = NONZERO	111	10011	CNEQ0
C16-23 = FF (ALL ONES)	011	10000	C1623EQFF
C21-22 = 0	010	10000	C2122EQ0
C24-27 = 1-9	110	00000	C2427EQNUM
C24-31 = FF (ALL ONES)	011	10001	C2431EQFF
C24-31 = NONZERO + SFF5 = 1	101	10000	C2431NEQ00F5
C26-29 = 0	011	10101	C2629EQ0
C28-31 = 0-9	110	00001	C2831EQDIG
C28-31 = B + D	110	00100	C2831EQMIN
(C28-31 = B + D) + (C28-31 = 9)* (P16-18 = 001)*(FF5 = 1)	010	10001	C2831EQNEG
(C28-31 = B + D) + (C28-31 = 9)* (P16-18 = 001)*(FF5 = 1)	101	10001	C2831EQNEG
C30-31 = 0	SC2	XX101	C3031EQ0
D00-01 = NONZERO	111	10101	D0001NEQ0
D00-02 = NONZERO	111	10110	D0002NEQ0
D00-31 = NONZERO + SFF1 = 1	010	01000	DNEQ00F1
D00-31 = NONZERO + SFF1 = 1	010	01001	DNEQ00F1
D00-31 = NONZERO + SFF2 = 1	SC2	XX001	OVFL2
D DIGITS SELECTED BY (109-12) = NONZERO	SC2	XX000	OVFL
EXECUTE FF = 1	000	00100	EXEC
FIXED DISC LOAD DEVICE	010	01101	FIXDISC
INITIAL PROGRAM LOAD	010	01100	IPL
INTERVAL TIMER INTERRUPT REQUEST	000	00010	TIRQ
I/O ACKNOWLEDGE	010	10010	ACK
I/O ACKNOWLEDGE	101	01001	ACK
I/O CONDITION CODE = 0 (I034-35 = 0)	010	10011	IOCCEQ0
IOST-1-15 = NONZERO (IOST ERROR)	000	01110	IOSTER
(I00-03=F+D) *OPERATION EXCEPTION	000	10011	ISSOPEX
(I01 = 1 + 112-15 = NONZERO)* CC COMPARE (BC/BCR)	010	00000	BCCOMP

Table 1-30. Sense Information Listed By Register (cont)

Register Description	Grp	Code	Mnemonic
I02 = 1	100	00000	I02EQ1
I03 = 1	001	00011	I03EQ1
I03 = 1	100	00011	I03EQ1
I05 = 0	111	01101	I05EQ0
I05 = 1	001	00000	I05EQ1
I06 = 0	011	01110	I06EQ0
I06 = 1	001	00101	I06EQ1
I06 = 1	010	10101	I06EQ1
I06 = 1	111	01011	I06EQ1
I06-07 = 01	011	01111	I0607EQ1
I07 = 0	001	00001	I07EQ0
(I07=0*(FF3 NOT EQ, FF4)* I07=1* (FF3 = FF4))*FF6=0	010	00001	RECOMP
I07 = 1	000	01010	I07EQ1
I07 = 1	001	00010	I07EQ1
I07 = 1	010	10110	I07EQ1
I07 = 1	100	00010	I07EQ1
I07 = 1	110	01101	I07EQ1
(I08=0*I10=0)*(I09=0*I10=1) (R! = 0-5, A,B)	101	00000	IR1EQL0
I08 = 1	011	00010	I08EQ1
I08 = 1 + I09-10 = 11 + I08-11 = 0 (R1 = 6-F, 0)	101	00011	IR1EQH1
I08-10 = 0 (R1=0 OR 1)	010	00011	IR1LT2
I08-11 = 0 (R1=0)	000	10000	IR1EQ0
I08-11 = 0 (R1=0)	011	01000	IR1EQ0
I08-11 = 0 (R1=0)	101	00100	IR1EQ0
I08-11 = 0 (R1=0)	110	00010	IR1EQ0
I08-11 = 0 + (SFF5=0) * (I12-15 = NONZERO)	SC2	XX100	IR1EQOD1
I08-11 = 0 & SFF5 = 1	110	10100	IR1EQOD2
I08-11 = I12-15 (R1=R2)	011	00100	IR1EQIR2
I08-14 = 0 * I15 = 1 (R = 1)	111	00001	IREQ1
I08-15 = 0 (R = 0)	110	00011	IREQ0
I08-15 = 0 (R = 0)	111	00101	IREQ0
(I08-15 = 0) + ((I08-15 = 1) * (SSF5 = 0))	111	01000	OP1LW
(I08-15 = 0)*(SFF2 = 0)*(SFF5=0)	111	01100	IREQONF25
I12-14 = 0 * I15 = 1 (R2=1)	010	00101	IR2EQ1
I12-14 = 0 * I15 = 1 (R2=1)	101	00101	IR2EQ1
I12-15 = 0 (R2=0)	010	00010	IR2EQ0
I12-15 = 0 (R2=0)	011	01001	IR2EQ0
I12-15 = 0 (R2=0)	110	00101	IR2EQ0
I12-15 = 0 + PSW16-18 = 001 (92-9300 MODE)	000	00000	IXEQ0
I12-15 = 0 + ((PSW16-18 = 001) * (I05-11 = 0))	101	00010	IR2EQ0ZAP
I12-15 = NONZERO (R2 NONZERO)	000	01000	IR2NEQ0
I13 = 1	011	00000	I13EQ1
I14 = 1	011	00011	I14EQ1
I15 = 1 + NOT PDECINTMR	011	00110	NRORS1

Table 1-30. Sense Information Listed By Register (cont)

Register Description	Grp	Code	Mnemonic
(I15 = 1 + (T00-23 = NONZERO)) * PDECINTMR	011	00111	RAT1S1
L00 = 0	100	01101	L00EQ0
L00 = 1	001	00110	L00EQ1
L00 = 1	011	10010	L00EQ1
L00 = 1	100	00110	L00EQ1
L00-07 = 64 (DECIMAL)	100	01011	L0007EQ40
L00-31 = 0	000	10010	LEQ0
L00-31 = 0	011	00101	LEQ0
(L00-31 = 0) * SFF2 = 1	011	10011	LEQ0AF2
L00-31 = NONZERO	001	01000	LNEQ0
L00-31 = NONZERO	011	01011	LNEQ0
L00-31 = NONZERO	100	01000	LNEQ0
(L00-31 = NONZERO) * (I01 = 1 + I12-15 = NONZERO)	000	00110	BCNTNEQ0
L01 = 1	100	01100	L01EQ1
L01 = 1 * (FF4 = 0 + (FF3 = 0 * FF6 = 1))	100	10110	FPDV
L01 = 1 * (FF4 = 0 + (FF3 NOT = FF6)) + FF3=1 * FF6=1	100	10111	FPMY
L01-07 = NONZERO	SC2	XX110	L010NEQ0
L01-07 GREATER THAN MANTISSA LENGTH	001	01101	LEXPDF
L01-31 = NONZERO	100	10001	L0131NEQ0
L03 = 1 + (L04 = 1 * L05-06 = NONZERO) (L03 - 07 > 9)	101	00110	L0307GT9
L07-09 = 0	001	01001	L0709EQ0
L08-11 = 0	001	10011	L0811EQ0
L08-11 = 0	100	10011	L0811EQ0
L08-31 = 0	111	10010	L0831EQ0
L08-31 = NONZERO	001	00111	L0831NEQ0
L08-31 = NONZERO	100	00111	L0831NEQ0
L11-14 = 0	100	01001	L1114EQ0
L12-15 = 0	001	01010	L1215EQ0
L16-19 = 0	100	01010	L1619EQ0
L16-31 = 0	000	01001	L1631EQ0
L16-31 = NONZERO	111	10001	L1631NEQ0
L24-31 = NONZERO	111	10000	L2431NEQ0
L28-31 = 0	011	10110	L2831EQ0
L30-31 = 0	011	10111	L3031EQ0
L31 = 1	010	10100	L31EQ1
L31 = 1	101	10100	L31EQ1
L31 = 1	110	00110	L31EQ1
MAR31 = 0	011	00001	M31EQ0
MAR31 = 1	111	00110	M31EQ1
PMENB0	100	00001	PMENB0
PMENB1	100	00100	PMENB1
PSW12 = 1	110	01011	P12EQ1
(PSW12 = 1) * (PSW16-18 = 001 OR 010)	010	10111	P12EQ1EM
(PSW12 = 1) * (PSW16-18 = 001 OR 010)	101	10111	P12EQ1EM

Table 1-30. Sense Information Listed By Register (cont)

Register Description	Grp	Code	Mnemonic
(PSW16-18 = 000 (NATIVE MODE) PSW16-18 = 001 OR 010 (EMULATION MODE)	110	00111	P1618EQ10R2
PSW16-18 = 010 (360/20 MODE)	000	00001	P1618EQ2
PSW34-35 = 11 (CONDITION CODE)	011	10100	P3435EQ3
PSW38 = 0 UNDERFLOW MASK BIT	001	10010	P38EQ0
PSW38 = 1 UNDERFLOW MASK BIT	100	10010	P38EQ1
PSW39 = 1 SIGNIFICANCE MASK BIT	001	00100	P39EQ1
SFF1 = 0	101	01010	FF1EQ0
SFF2 = 0	SC2	XX010	FF2EQ0
(SFF2 = 1) * SFF3 = 0) * (SFF4 = 1)	111	00011	FF234EQ101
SFF3 = 0	010	00111	FF3EQ0
SFF3 = 0	101	00111	FF3EQ0
SFF3 = 0	110	01001	FF3EQ0
SFF3 = 0	111	01001	FF3EQ0
(SFF3 = 1) * (SFF5 = 0) * (SFF6 = 0)	101	10101	FF356EQ100
SFF3 = SFF4	101	10110	FF3EQFF4
SFF3 NOT EQUAL SFF4	010	00100	FF3NEQFF4
SFF3 NOT EQUAL SFF4	111	00000	FF3NEQFF4
SFF4 = 0	110	01010	FF4EQ0
SFF4 = 0	111	01010	FF4EQ0
SFF6 = 1	110	01000	FF6EQ1
SFF6 = 1 + L00 = 1 * (SFF4 = 0 + (L01-31 = NONZERO)	110	10010	OVFLCVB
SYNCHFF = 1 * NO INTERVAL TIMER INTERRUPT REQUEST	000	00101	NITASC
SYSTEM RESET FLIP-FLOP = 0	110	10001	NSRFF
X00 = 1	100	10101	X00EQ1
X00-05 = 0	111	10111	X0005EQ0
X00-07 = 0	011	01010	XEQ0
X00-07 = 0	111	00010	XEQ0
X00-07 = 1	100	01111	XRW01
X00-07 = 15 (DECIMAL)	100	00101	XEQ0F
X00-07 = ALL ONES	001	01011	XEQFF
X00-07 = NONZERO	101	01000	XNEQ0
X01-07 = 0	001	10000	X0107EQ0
X01-07 = 0	100	10000	X0107EQ0
X06-07 = 11	SC2	XX111	X0607EQ3
X07 = 1	110	01110	X07EQ1
Z00 = 0	011	01101	Z00EQ0
Z00 = 1	000	01011	Z00EQ1
Z00-01 = NONZERO	000	10001	Z0001NEQ0
Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 OR 010))	000	00011	ZBEQ0
Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 OR 010))	010	01111	ZBEQ0
Z00-3 = 0 + (Z00 = 0 * (PSW16-18 = 001 OR 010))	101	01111	ZBEQ0
Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 OR 010))	110	01111	ZBEQ0

Table 1-30. Sense Information Listed By Register (cont)

Register Description	Grp	Code	Mnemonic
Z00-03 = 0 + (Z00 = 0 * (PSW16-18 = 001 OR 010))	111	01111	ZBEQ0
(Z00-07 NOT 0)*(SFF4=0) + (Z08-15 NOT 0)*(SFF4=1))* IO7=1	110	01100	ZTEST
Z01 = 1	000	01100	Z01EQ1
Z06-15 = 1	000	01111	Z0615EQ1
Z BYTE (SSF1) = DIGIT SELECT OR SIGNIFICANCE START	110	10011	ZPAT1
Z BYTE (SSF1) = DIGIT SELECT OR FIELD SEPARATOR	SC2	XX011	ZPAT2

NOTES:

1. Sense conditions consisting of a bit or a field of a register are given mnemonics in a standard format rnnmmNEQv. The first letter r identifies the register; valid entries are:

A (Adder)	M (MAR)
C (Control Reg.)	P (PSW)
D (Decimal Correct)	T (Timer)
F (Sense Flip-Flop)	W (Write Data Register)
I (Instr. Reg.)	X (Utility Counter)
L (Latch)	Z (Read Data Register)

2. GRP (group) column refers to the contents of bits 1-3 of the SAB field of the current BDW (bit Ø is not implemented), and the CODE column refers to the contents of the SNSC field of the current microinstruction.

3. The two decimal digits nn identify the single bit, or the leftmost bit of the field, being tested. If only one bit is tested, mm is omitted; otherwise these two decimal digits identify the rightmost bit of the field. If the field consists of the entire register, both nn and mm are omitted. The letters EQ (equals) or NEQ (not equals) are followed by a hexadecimal value v. Either EQØ or EQ1 are used when referring to a single bit.

Table 1-31. Program Exception Equations INT Statements

	PX GROUP	INT CODE	Mnemonic	Description
GROUP Ø	000	000	MSTORE	ANY MAIN STORE ERROR
	000	001	DWB	MAR29 + MAR30 + MAR31
	000	010	FWB	MAR30 + MAR31
	000	011	HWB	MAR31
	000	100	R10DD	I11
	000	101	IMOREE	NATIVEMD * $\overline{I00}$ * $\overline{I01}$ * $\overline{I13}$ * I14 +36020MD * $\overline{I00}$ * $\overline{I01}$ * $\overline{I03}$ * $\overline{I04}$ * $\overline{I06}$ * $\overline{I08}$ +36020MD * $\overline{I00}$ * $\overline{I01}$ * $\overline{I03}$ * $\overline{I12}$ * (I13 + I14 + I15) +36020MD * $\overline{I00}$ * $\overline{I01}$ * I03 * ($\overline{I08}$ + $\overline{I12}$) +36020MD * $\overline{I00}$ * I01 * (I04 + $\overline{I05}$ + $\overline{I06}$ + $\overline{I07}$) * $\overline{I08}$ +36030MD * $\overline{I00}$ * $\overline{I01}$ * (I12 + I13 + I14 + I15)
	000	110	FXOVF	NATIVEMD * PSW36 * $\overline{I00}$ * UFOVF1 +NATIVEMD * PSW36 * I00 * $\overline{I03}$ * $\overline{UFOVF2}$ +NATIVEMD * PSW36 * I00 * $\overline{I02}$ * $\overline{I03}$ * SFF3 +36020MD * UFOVF2
	000	111	FXDIV	SFF5
GROUP 1	001	000	MSTORE	ANY MAIN STORE ERROR
	001	001	DWB	MAR29 + MAR30 + MAR31
	001	010	FWB	MAR30 + MAR31
	001	011	SIGNIF	SFF5
	001	100	R12ODD	I08 + I11 + $\overline{I01}$ * (I12 + I15)
	001	101	EXPUNF	SFF5
	001	110	EXPOVF	SSF5
	001	111	FLDIV	SFF5

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Table 1-31. Program Exception Equations INT Statements (cont)

PX GROUP	INT CODE	Mnemonic	Description
010	000	MSTORE	ANY MAIN STORE ERROR
010	001	DWB	MAR29 + MAR30 + MAR31
010	010	QWB	MAR28 + MAR29 + MAR30 + MAR31
010	011	DIGIT	$(\overline{929300MD} + IO5 + IO6 + IO7) * C00 * (C01 + C02)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C04 * (C05 + C06)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C06 * (C09 + C10)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C12 * (C13 + C14)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C16 * (C17 + C18)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C20 * (C21 + C22)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C24 * (C25 + C26)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C28 * (C29 + C30)$
GROUP 2			
010	100	SIGN	$929300MD * (\overline{C28} + (\overline{C29} * \overline{C30}))$
010	101	IOSTSRER	ANY MAIN STORE ERROR (FOR IOST)
010	110	CSWADR	C16 + C17 + C18 + C19 + C20
010	111	FXDIV	SFF5
011	000	MSTORE	ANY MIAN STORE ERROR
011	001	L2GT7	IO5 * L28
011	010	L1LEL2	$IO5 * (\overline{COR00} + \overline{L28} * \overline{L29} * \overline{L30} * \overline{L31}) + 36020MD * COR00$
011	011	DIGIT	$(\overline{929300MD} + IO5 + IO6 + IO7) * C00 * (C01 + C02)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C04 * (C05 + C06)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C08 * (C09 + C10)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C12 * (C13 + C14)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C16 * (C17 + C18)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C20 * (C21 + C22)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C24 * (C25 + C26)$ $+ (\overline{929300MD} + IO5 + IO6 + IO7) * C28 * (C29 + C30)$
GROUP 3			
011	100	SIGN	$929300MD * (C28 + (C29 * C30))$

Table 1-31. Program Exception Equations INT Statements (cont)

	PX GROUP	INT CODE	Mnemonic	Description
	011	101	LZEROS	(L03-07 = 0-7) * (C00-07 = NONZERO) + (L03-07 = 0-5) * (C08-15 = NONZERO) + (L03-07 = 0-3) * (C16-23 = NONZERO) + (L03-07 = 0-1) * (C24-31 = NONZERO)
GROUP 3	011	110	DECOVF	PSW37 * $\overline{I06}$ * $\overline{I07}$ * SFF5 + PSW37 * (I06 + I07) * (SFF2 + $\overline{(\overline{SFF5} * SFF6)}$
(cont)	011	111	DECDIV	CORD00 * $\overline{SFF6}$

NOTES:

1. The PX-GRP column refers to the contents of bit Ø-2 of the PX field of the current BDW, and the INT-CODE columns refers to the contents of the INT field of the current microinstruction.

2. Bit Ø of the PX field is not implemented. (Only four groups are available.)

3. If the specified equation is true (having a value of logical one), a program-exception interrupt request will be initiated.

4. Most of the terms in these logic equations refer to bit positions of registers in the CPU data path and are, therefore, self-explanatory. Other terms are defined as follows:

UFOVF1 = COR00 * $\overline{COUT01}$ + $\overline{COR00}$ * COUT01
UFOVF2 = COR16 * $\overline{COUT17}$ + $\overline{COR16}$ * COUT17
NATIVEMD = PSW16-18 = 000
929300MD = PSW16-18 = 001
36020MD = PSW16-18 = 010
COR = CARRY-OUT REGISTER

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COMPANY CONFIDENTIAL
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Table 1-32. COS Allocations

Location*	Usage
000	System Reset Routine Entry
001-0FF	Instruction BDW (and normal Microcoding)
100	Staticise Entry (Microword WA0000)
101	Machine Check Interrupt Entry 1
102	Program Exception Interrupt Entry
103	Interval Timer Interrupt Entry
104	IOST Tabling Entry
105	IOST Interrupt Entry
106	Monitor Interrupt Entry
107	IOST Non-Recoverable Error Entry
108	Machine Check Interrupt Entry 2
10A-10B	IPL Entry
300	Diagnostic Sub. Functions Entry
310	Softscope Instruction Entry
311-380	Transient Area
3FF	ILCS Exit (Systems with 1K COS, without F.P.)
600-7FE	Transient Area
7FF	ILCS Exit (Systems with 2K COS, with F.P.)
—	———
800-8FF	Read Only Memory

* Hexadecimal

Table 1-33. COS Chip Locations (1K-2K)

COS* ADDRESS RANGE - 000 to 3FF			
Micro-inst. Bit	COS Bit	Board Loc.	Chip Co-ord.
SA00	01	51AB06	97U2
SA01	02	51AB06	87U2
SA02	03	51AB06	77U2
SB00	04	51AB06	68U2
SB01	05	51AB06	58U2
SB02	06	51AB06	48U2
S00	07	51AB06	38U2
S01	09	51AB08	97U2
S02	10	51AB08	87U2
S03	11	51AB08	77U2
S04	12	51AB08	68U2
AAD0	13	41AB08	58U2
AAD1	14	51AB08	48U2
AAD2	15	51AB08	38U2
AAD3	17	51AB06	97R6
AWE00	18	51AB06	87R6
AWE01	19	51AB06	77R6
AWE02	20	51AB06	68R6
BAD0	21	51AB06	58R6
BAD1	22	51AB06	48R6
BAD2	23	51AB06	38R6
BAD3	25	51AB08	97R6
BWE00	26	51AB08	87R6
BWE01	27	51AB08	77R6
BWE02	28	51AB08	68R6
BWE03	29	51AB08	58R6
H00	30	51AB08	48R6
H01	31	51AB08	38R6
BWAD0	33	51AB06	97P2
BWAD1	34	51AB06	87P2
BWAD2	35	51AB06	77P2
BWAD3	36	51AB06	68P2
M00	37	51AB06	58P2
M01	38	51AB06	48P2
M02	39	51AB06	38P2
PTY00	41	51AB08	97P2
SC00	42	51AB08	87P2
SC01	43	51AB08	77P2
SC02	44	51AB08	68P2

*90/30 COS BOARDS (3621699-02)

Table 1-33. COS Chip Locations (1K-2K) (cont)

COS* ADDRESS RANGE - 000 to 3FF

Micro-inst. Bit	COS Bit	Board Loc.	Chip Co-ord.
F00	45	51AB08	58P2
F01	46	51AB08	48P2
F02	47	51AB08	38P2
CAR00	49	51AB06	97L4
CAR01	50	51AB06	87L4
DA00	51	51AB06	77L4
DA01	52	51AB06	68L4
DA02	53	51AB06	58L4
DB00	54	51AB06	48L4
DB01	55	51AB06	38L4
DB02	57	51AB08	97L4
SNSC0	58	51AB08	87L4
SNSC1	59	51AB08	77L4
SNSC2	60	51AB08	68L4
SNSC3	61	51AB08	58L4
SNSC4	62	51AB08	48L4
SNSF0	63	51AB08	33L4
SNSF1	65	51AB06	97H6
SNSF2	66	51AB06	87H6
INT00	67	51AB06	77H6
INT01	68	51AB06	68H6
INT02	69	51AB06	58H6
MISC0	70	51AB06	48H6
MISC1	71	51AB06	38H6
MISC2	73	51AB08	97H6
MISC3	74	51AB08	87H6
MISC4	75	51AB06	77H6
MISC5	76	51AB08	68H6
MK00	77	51AB08	58H6
JC00	78	51AB08	48H6
JC01	79	51AB08	38H6
JC01	81	51AB06	97F2
PTY01	82	51AB06	87F2
Not Used	83	51AB06	77F2

*90/30 COS BOARDS (3621699-02)

Table 1-33. COS Chip Locations (1K-2K) (cont)

Micro-inst. Bit	COS Bit	Board Loc.	Chip Co-ord.
COS* ADDRESS RANGE - 000 to 3FF			
E00	84	51AB06	68F2
E01	85	51AB06	58F2
E02	86	51AB06	48F2
E03	87	51AB06	38F2
E04	89	51AB08	97F2
E05	90	51AB08	87F2
E06	91	51AB08	77F2
E07	92	51AB08	68F2
ED00	93	51AB08	58F2
ED01	94	51AB08	48F2
ED02	95	51AB08	38F2
ADDRESS RANGE - 400 to 7FF			

The chip coordinates preceding may be used with the exception that board location 51AB06 will be 51AB10 and board location 51AB08 will be 51AB12.

Table 1-34. COS IC Locations (4K)

Micro-inst. Bit	COS Bit	Board Loc.	IC Co-ord
SA00	01	64AB04	126P
SA01	02		126L2
SA02	03		126F
SB00	04		126J
SB01	05		120L2
SB02	06		120P
S00	07		120F
S01	09		120J
S02	10		112J
S03	11		112L2
S04	12		112P
AAD00	13		106J
AAD01	14		106L2
AAD02	15		106P
AAD03	17		96P
AWE00	18		90P
AWE01	19		84P
AWE02	20		78P
BAD00	21		72P
BAD01	22		66P
BAD02	23		60P
BAD03	25		54P
BWE00	26		48P
BWE01	27		42P
BWE02	28		36P
BWE03	29		30P
H00	30		24P
H01	31		18P
W00	33		96L2
W01	34		90L2
SM00	35		84L2
SM01	36		78L2
M00	37		72L2
M01	38		66L2
M02	39		60L2
PTY00	41		54L2
SC00	42		48L2
SC01	43		42L2
SC02	44	64AB04	36L2

Table 1-34. COS IC Locations (4K)(cont)

Micro-inst. Bit	COS Bit	Board Loc.	IC Co-ord
F00	45	64AB04	30L2
F01	46		24L2
F02	47		18L2
CAR00	49		96J
CAR01	50		90J
DA00	51		84J
DA01	52		78J
DA02	53		72J
DB00	54		66J
DB01	55		60J
DB02	57		54J
SNSC00	58		48J
SNSC01	59		42J
SNSC02	60		36J
SNSC03	61		30J
SNSC04	62		24J
SNSF00	63		18J
SNSF01	65		96F
SNSF02	66		90F
INT00	67		84F
INT01	68		78F
INT02	69		72F
MISC00	70		60F
MISC01	71		54F
MISC02	73		48F
MISC03	74		42F
MISC04	75		36F
MISCSL	76		66F
MK00	77		30F
JC00	78		24F
JC01	79		18F
JC02	81		96C6
PTY01	82		90C6
Not Used	83	64AB04	84C6

Table 1-34. COS IC Locations (4K)(cont)

Micro-inst. Bit	COS Bit	Board Loc.	IC Co-ord
E00	84	64AB04	78C6
E01	85		72C6
E02	86		66C6
E03	87		60C6
E04	89		54C6
E05	90		48C6
E06	91		42C6
E07	92		36C6
ED00	93		30C6
ED01	94		24C6
ED02	95	64AB04	18C6

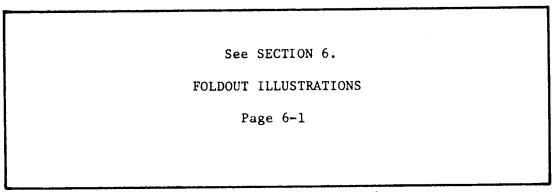


Figure 1-7. Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-00,-01,-02,-03 90/30)(Sheet 1 of 2)

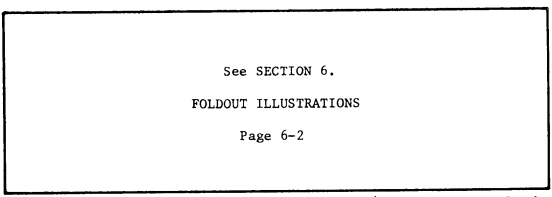


Figure 1-7. Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-00,-01,-02,-03 90/30)(Sheet 2 of 2)

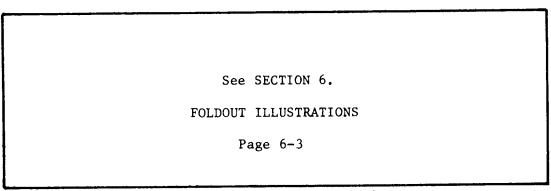


Figure 1-8. Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-02,-03 90/25 and 90/30B) (Sheet 1 of 2)

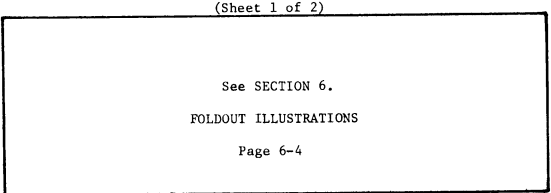


Figure 1-8. Initial Load of Control Storage/Initial Program Load General Operational Sequence (3029-02,-03 90/25 and 90/30B) (Sheet 2 of 2)

Table 1-35. I/O Channel Number Assignments

CHANNEL NO.	ASSIGNMENTS	PHYSICAL LOCATION
0	Integrated Peripheral Channel (IPC)	Processor Cabinet
1	Multiplexer Channel	Expansion Cabinet
2	Not Assigned	- - -
3	Integrated Disc Adapter (IDA)	Processor Cabinet
4	Selector Channel 1	Expansion Cabinet
5	Communications Channel	Communication Cabinet
6	Selector Channel 2	Expansion Cabinet
7	I/O Status Tabler	Processor Cabinet

SECTION 2

STORAGE

Bit 9-10 i mem modül.

SAC	BYTE Ø	BYTE 1
0	A08	A07
1	A06	A05
2	A04	A03
3	A02	A01

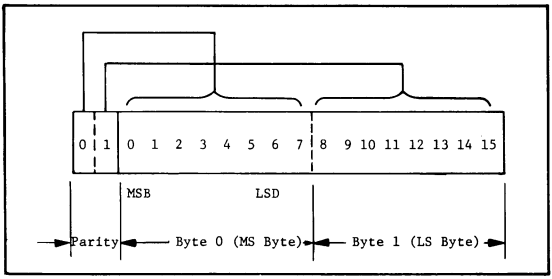


Figure 2-1. Memory Data Format

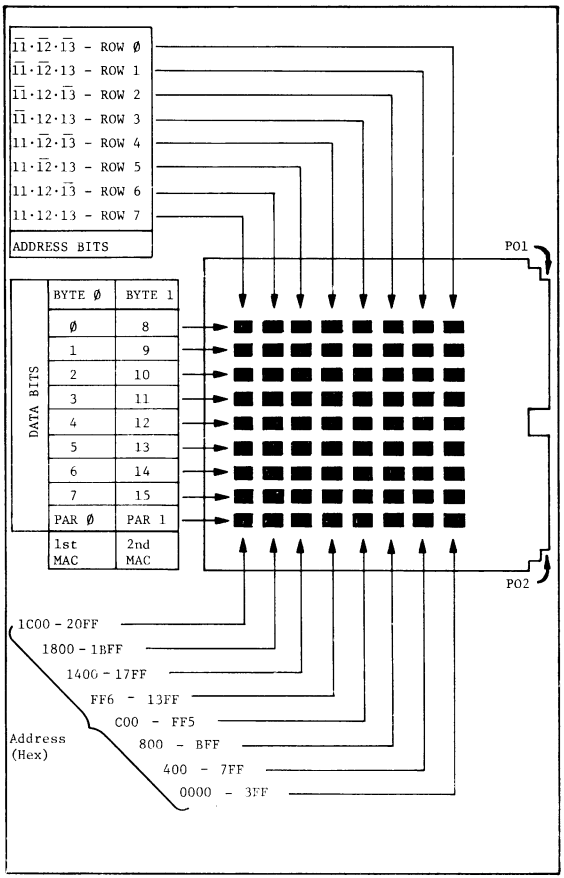


Figure 2-2. 7024 Memory Array Card (3029-00, -01 90/30 - Serial Numbers Below 746 or J326)

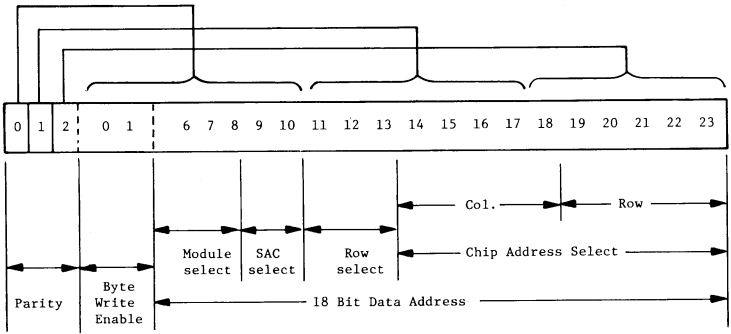

0 1 2 0 1 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
Col.
Row
Module select
SAC select
Row select
Chip Address Select
Parity
Byte Write Enable
18 Bit Data Address
Byte Write Enable
00 - Read Halfword
01 - Write L.S. Byte
10 - Write M.S. Byte
11 - Write Halfword

Figure 2-3. 7024 Memory Address Format (3029-00, -01 90/30 - Serial Numbers Below 746 or J326)

Table 2-1. 7024 Memory Interface Signal Connections
(3029-00, -01 90/30 Serial Numbers
Below 746 or J326)

Signal	Connector					
	Pin	Module	Interface Assy A06A02			
			Mod 0	Mod 1	Mod 2	Processor
Initiate	-02	J10J01	J01A	J01B	J01C	J01L
Refresh	-05					
Write data Bit 0	-08					
1	-11					
2	-14					
3	-17					
4	-20					
5	-23					
6	-26					
7	-29					
8	-32					
9	-35					
10	-38	J10J01	J01A	J01B	J01C	J01L
11	-02	J10J02	J02A	J02B	J02C	J02L
12	-05					
13	-08					
14	-11					
Write data Bit15	-14					
Write par.Byte 0	-17					
Write par.Byte 1	-20					
Byte write cont0	-23					
Byte write cont1	-26					
Write abort	-29					
Master clear	-32					
Storage hold cont.	-35					
Par.check disable	-38	J10J02	J02A	J02B	J02C	J02L

Table 2-1. 7024 Memory Interface Signal Connections
(3029-00, -01 90/30 Serial Numbers
Below 746 or J326)(cont)

Signal	Connector					
	Pin	Module	Interface Assy A06A01			
			Mod 0	Mod 1	Mod 2	Processor
Address Accept	-02	J10J05	J02A	J02B	J02C	J02L
Address par chk.	-05	↕	↕	↕	↕	↕
Data par chk.	-08	↕	↕	↕	↕	↕
Storage hold	-11	↕	↕	↕	↕	↕
High temperature	-14	↕	↕	↕	↕	↕
Test mode	-17	↕	↕	↕	↕	↕
On Line	-20	↕	↕	↕	↕	↕
Read data Bit 0	-23	↕	↕	↕	↕	↕
↕ 1	-26	↕	↕	↕	↕	↕
↕ 2	-29	↕	↕	↕	↕	↕
↕ 3	-32	↕	↕	↕	↕	↕
↕ 4	-35	↕	↕	↕	↕	↕
Read data Bit 5	-38	J10J05	J02A	J02B	J02C	J02L
Read data Bit 6	-02	J10J06	J03A	J03B	J03C	J03L
↕ 7	-05	↕	↕	↕	↕	↕
↕ 8	-08	↕	↕	↕	↕	↕
↕ 9	-11	↕	↕	↕	↕	↕
↕ 10	-14	↕	↕	↕	↕	↕
↕ 11	-17	↕	↕	↕	↕	↕
↕ 12	-20	↕	↕	↕	↕	↕
↕ 13	-23	↕	↕	↕	↕	↕
↕ 14	-26	↕	↕	↕	↕	↕
Read data Bit 15	-29	↕	↕	↕	↕	↕
Read par Bit 0	-32	↕	↕	↕	↕	↕
Read par Bit 1	-35	↕	↕	↕	↕	↕
Not used	-38	J10J06	J03A	J03B	J03C	J03L

Table 2-1. 7024 Memory Interface Signal Connections (3029-00, -01 90/30 Serial Numbers Below 746 or J326)(cont)

Signal	Pin	Module	Connector: Interface Assy A06A02 Mod 0	Mod 1	Mod 2	Processor
Address Bit 23	-02	J10J03	J03A	J03B	J03C	J03L
22	-05					
21	-08					
20	-11					
19	-14					
18	-17					
17	-20					
16	-23					
15	-26					
14	-29					
13	-32					
12	-35					
Address Bit 11	-38	J10J03	J03A	J03B	J03C	J03L

Signal	Pin	Module	Connector: Interface Assy A06A01 Mod 0	Mod 1	Mod 2	Processor
Address Bit 10	-02	J10J04	J01A	J01B	J01C	J01L
09	-05					
08	-08					
07	-11					
Address Bit 06	-14					
Address par Bit 0	-17					
Address par Bit 1	-20					
Address par Bit 2	-23					
Not Used	-26					
	-29					
	-32					
	-35					
Not Used	-38	J10J04	J01A	J01B	J01C	J01L

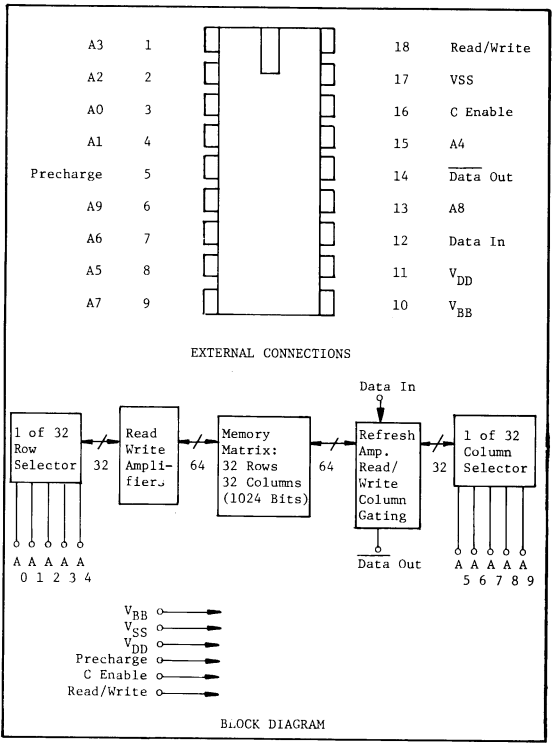


Figure 2-4. 1103 Chip Description For 7024 Memory
(3029-00, -01 90/30 - Serial Numbers
Below 746 or J326)

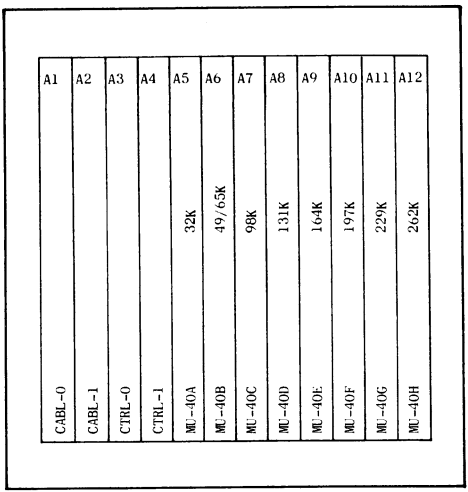


Figure 2-5. MU40 Storage Unit (3029-00, -01 90/30)

Table 2-2. MU40 Selection via ADRS 07-09 (3029-00, -01 90/30)

ADDRESS BITS			MU	CARD CAGE	ADDRESS RANGE HEX			
					MODULE 1		MODULE 2	
07	08	09	SELECTED	LOCATION	FROM	TO	FROM	TO
OFF	OFF	OFF	A	SLOT 5	00000	07FFF	40000	47FFF
OFF	OFF	ON	B	SLOT 6	08000	0FFFF	48000	4FFFF
OFF	ON	OFF	C	SLOT 7	10000	17FFF	50000	57FFF
OFF	ON	ON	D	SLOT 8	1800	1FFFF	58000	5FFFF
ON	OFF	OFF	E	SLOT 9	20000	27FFF	60000	67FFF
ON	OFF	ON	F	SLOT 10	28000	2FFFF	68000	6FFFF
ON	ON	OFF	G	SLOT 11	30000	37FFF	70000	77FFF
ON	ON	ON	H	SLOT 12	38000	3FFFF	78000	7FFFF

Table 2-3. MU40 Card Column Selection Via ADRS 10-11 (3029-00, -01 90/30)

Address Bits 10	11	Card Column Selected	Memory Address (X = DON'T CARE)
OFF	OFF	A	X0XXX, X1XXX, X8XXX, X9XXX
OFF	ON	E	X2XXX, X3XXX, XAXXX, XBXXX
ON	OFF	B	X4XXX, X5XXX, XCXXX, XDXXX
ON	ON	F	X6XXX, X7XXX, XEXXX, XFXXX

The location of the columns on the card is shown in figure 2-6.

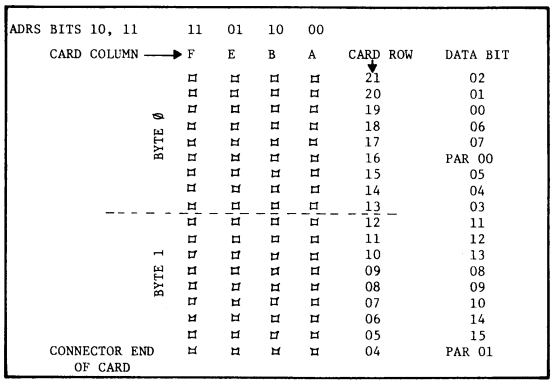


Figure 2-6. Memory Chip Layout on MU40 (3029-00, -01 90/30)

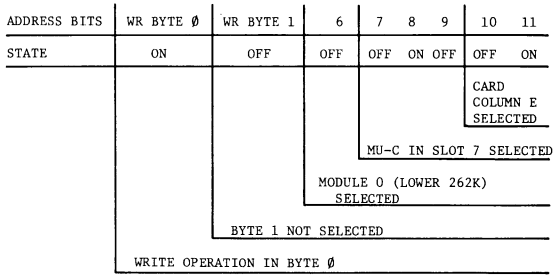
The failing data bit may be identified from the secondary error displays of the diagnostic programs (DH4108) or by executing continuous write and read instructions from the maintenance panel at the address at which the error occurred.

Table 2-4. MU40 Data Bit Locations
(3029-00, -01 90/30)

Memory Data Bit	Card Row Location	Write Data Pin Nos.	Read Data Pin Nos.	CPU Reference Bit No.
		MU	MU	
Lower 00	19	25	62	00
Lower 01	20	23	64	01
Lower 02	21	21	66	02
Lower 03	13	43	42	03
Lower 04	14	41	44	04
Lower 05	15	39	46	05
Lower 06	18	27	26	06
Lower 07	17	29	28	07
Lower 08	16	31	32	PAR 00
Upper 00	9	55	60	08
Upper 01	8	57	58	09
Upper 02	7	59	56	10
Upper 03	12	45	40	11
Upper 04	11	47	38	12
Upper 05	10	49	36	13
Upper 06	6	61	24	14
Upper 07	5	63	22	15
Upper 08	4	67	20	PAR 01

EXAMPLE:

The memory system halts at the following address, with failing data bit 05.



The failing chip is seen to be located in the Lower 262K system, on MU-C, in slot 7. It is in card column E, card row 15.

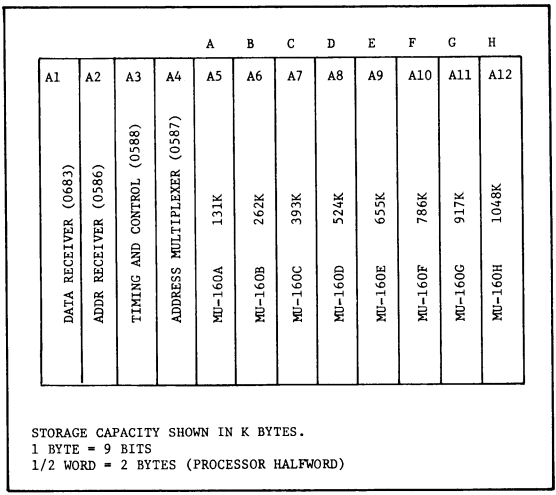


Figure 2-7. MU160 Fully Populated Storage Unit (1048K Bytes) (3029-02, -03 90/25, 90/30, and 90/30B)

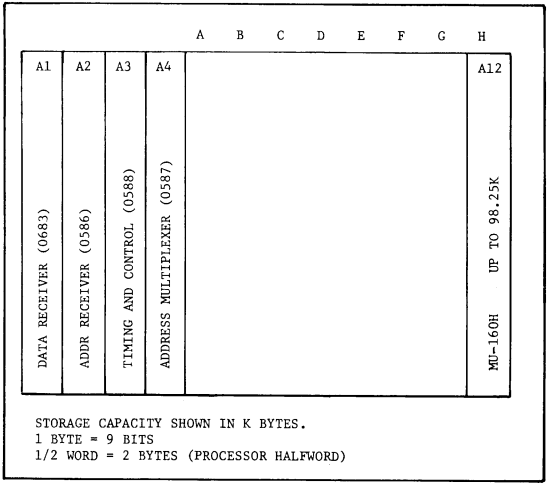


Figure 2-8. MU160 Partially Populated Storage Unit (98.25K Bytes Maximum) (3029-02, -03 90/25, 90/30, and 90/30B)

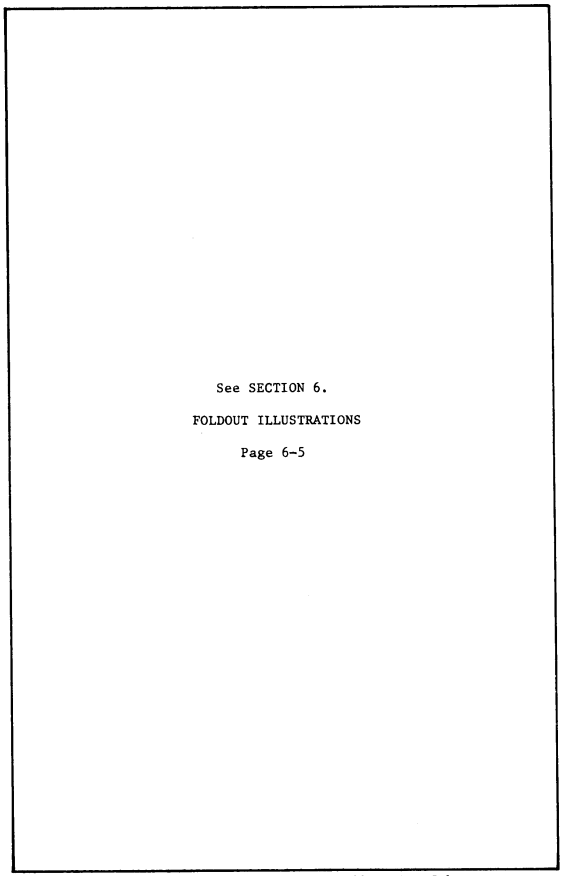


Figure 2-9. MU160 Main Storage Addressing Scheme (3029-02, -03 90/25, 90/30, and 90/30B)

Table 2-5. MU160 Address Decoding
(3029-02, -03 90/25, 90/30, and 90/30B)

Address Range Hex		MU160 Selected		Memory Block Selected	Card Cage Location		12	13	14	MAR
From	To	Norm	PP*		Norm	PP*	5	6	7	1/0
0 0 0 0 0	0 7 F F F	A	H	0	A5	A12	0	0	0	
0 8 0 0 0	0 F F F F	A	H	1	A5	A12				
1 0 0 0 0	1 7 F F F	A	H	2	A5	A12				
1 8 0 0 0	1 F F F F	A	H	3	A5					
2 0 0 0 0	2 7 F F F	B	H	0	A6	A12	0	0	1	
2 8 0 0 0	2 F F F F	B	H	1	A6	A12				
3 0 0 0 0	3 7 F F F	B	H	2	A6	A12				
3 8 0 0 0	3 F F F F	B		3	A6					
4 0 0 0 0	4 7 F F F	C	H	0	A7	A12	0	1	0	
4 8 0 0 0	4 F F F F	C	H	1	A7	A12				
5 0 0 0 0	5 7 F F F	C	H	2	A7	A12				
5 8 0 0 0	5 F F F F	C		3	A7					
6 0 0 0 0	6 7 F F F	D	H	0	A8	A12	0	1	1	
6 8 0 0 0	6 F F F F	D	H	1	A8	A12				
7 0 0 0 0	7 7 F F F	D	H	2	A8	A12				
7 8 0 0 0	7 F F F F	D		3	A8					
8 0 0 0 0	8 7 F F F	E	H	0	A9	A12	1	0	0	
8 8 0 0 0	8 F F F F	E	H	1	A9	A12				
9 0 0 0 0	9 7 F F F	E	H	2	A9	A12				
9 8 0 0 0	9 F F F F	E		3	A9					
A 0 0 0 0	A 7 F F F	F	H	0	A10	A12	1	0	1	
A 8 0 0 0	A F F F F	F	H	1	A10	A12				
B 0 0 0 0	B 7 F F F	F	H	2	A10	A12				
B 8 0 0 0	B F F F F	F		3	A10					
C 0 0 0 0	C 7 F F F	G	H	0	A11	A12	1	1	0	
C 8 0 0 0	C F F F F	G	H	1	A11	A12				
D 0 0 0 0	D 7 F F H	G	H	2	A11	A12				
D 8 0 0 0	D F F F F	G		3	A11					
E 0 0 0 0	E 7 F F F	H		0	A12		1	1	1	
E 8 0 0 0	E F F F F	H		1	A12					
F 0 0 0 0	F 7 F F F	H		2	A12					
F 8 0 0 0	F F F F F	H		3	A12					

*PP = With Partially-Populated Card

Table 2-6. MU160 Jumper Installation
(3029-02, -03 90/25, 90/30, and 90/30B)

Configuration	MU160's							
	A	B	C	D	E	F	G	H
1. 0-32.75K								W2
2. 0-65.50K								W2,W3
3. 0-98.25K								W2,W1,W3
4. 0-131K	W1							
5. 0-163.75K	W1							W2
6. 0-196.50K	W1							W2,W3
7. 0-229.25K	W1							W2,W1,W3
8. 0-262K	W1	W1						
9. 0-294.75K	W1	W1						W2
10. 0-327.50K	W1	W1						W2,W3
11. 0-360.25K	W1	W1						W2,W1,W3
12. 0-393K	W1	W1	W1					
13. 0-425.75K	W1	W1						W2
14. 0-458.50K	W1	W1	W1					W2,W3
15. 0-491.25K	W1	W1	W1					W2,W1,W3
16. 0-524K	W1	W1	W1	W1				
17. 0-556.75K	W1	W1	W1	W1				W2
18. 0-589.50K	W1	W1	W1	W1				W2,W3
19. 0-622.25K	W1	W1	W1	W1				W2,W1,W3
20. 0-655K	W1	W1	W1	W1	W1			
21. 0-687.75K	W1	W1	W1	W1	W1			W2
22. 0-720.50K	W1	W1	W1	W1	W1			W2,W3
23. 0-753.25K	W1	W1	W1	W1	W1			W2,W1,W3
24. 0-786K	W1	W1	W1	W1	W1	W1		
25. 0-818.75K	W1	W1	W1	W1	W1	W1		W2
26. 0-851.50K	W1	W1	W1	W1	W1	W1		W2,W3
27. 0-884.25K	W1	W1	W1	W1	W1	W1		W3,W1,W3
28. 0-917K	W1	W1	W1	W1	W1	W1	W1	
29. 0-949.75K	W1	W1	W1	W1	W1	W1	W1	W2
30. 0-982.50K	W1	W1	W1	W1	W1	W1	W1	W2,W3
31. 0-1015.25K	W1	W1	W1	W1	W1	W1	W1	W2,W1,W3
32. 0-1048K	W1	W1	W1	W1	W1	W1	W1	W1

Table 2-7. MU160 Interface Pin Assignments (3029-02, -03 90/25, 90/30, and 90/30B)

DATA RECEIVER CARD		
Connector-Pin No.	Signal Name	Level
J01- 8	WRITE DATA 00	L
J01-11	WRITE DATA 01	L
J01-14	WRITE DATA 02	L
J01-17	WRITE DATA 03	L
J01-20	WRITE DATA 04	L
J01-23	WRITE DATA 05	L
J01-26	WRITE DATA 06	L
J01-29	WRITE DATA 07	L
J01-32	WRITE DATA 08	L
J01-35	WRITE DATA 09	L
J01-38	WRITE DATA 10	L
J02- 2	WRITE DATA 11	L
J02- 5	WRITE DATA 12	L
J02- 8	WRITE DATA 13	L
J02-11	WRITE DATA 14	L
J02-14	WRITE DATA 15	L
J02-17	WRITE PARITY BYTE 0	L
J02-20	WRITE PARITY BYTE 1	L
J01- 2	CYCLE INITIATE	L
J01- 5	REFRESH ACTUATE	L
J02-23	BYTE WRITE ENABLE 0	H
J02-26	BYTE WRITE ENABLE 1	H
J02-29	WRITE ABORT	H
J02-32	SYSTEM RESET	L
J02-35	STORAGE HOLD CONTROL	L
J02-38	PARITY CHECK DISABLE	H
J05- 2	ADDRESS ACCEPT	L
J05- 5	ADDRESS PARITY CHECK	L
J05- 8	DATA PARITY CHECK	L
J05-11	STORAGE HOLD	L
J05-23	READ DATA 0	L
J05-26	READ DATA 1	L
J05-29	READ DATA 2	L
J05-32	READ DATA 3	L
J05-35	READ DATA 4	L
J05-38	READ DATA 5	L
J05-14,17,20	SPARES	

Table 2-7. MU160 Interface Pin Assignments (3029-02, -03 90/25, 90/30, and 90/30B)(cont)

ADDRESS RECEIVER CARD

Connector-Pin No.	Signal Name	Level
J04-26	ADDRESS 05	H
J04-14	ADDRESS 06	H
J04-11	ADDRESS 07	H
J04- 8	ADDRESS 08	H
J04- 5	ADDRESS 09	H
J04- 2	ADDRESS 10	H
J03-38	ADDRESS 11	H
J03-35	ADDRESS 12	H
J03-32	ADDRESS 13	H
J03-29	ADDRESS 14	H
J03-26	ADDRESS 15	H
J03-23	ADDRESS 16	H
J03-20	ADDRESS 17	H
J03-17	ADDRESS 18	H
J03-14	ADDRESS 19	H
J03-11	ADDRESS 20	L
J03- 8	ADDRESS 21	L
J03- 5	ADDRESS 22	L
J03- 2	ADDRESS 23	L
J04-17	ADDRESS PARITY BIT 0	L
J04-20	ADDRESS PARITY BIT 1	L
J04-23	ADDRESS PARITY BIT 2	L
J06- 2	READ DATA 6	L
J06- 5	READ DATA 7	L
J06- 8	READ DATA 8	L
J06-11	READ DATA 9	L
J06-14	READ DATA 10	L
J06-17	READ DATA 11	L
J06-20	READ DATA 12	L
J06-23	READ DATA 13	L
J06-26	READ DATA 14	L
J06-29	READ DATA 15	L
J06-32	READ PARITY BYTE 0	L
J06-35	READ PARITY BYTE 1	L
J06-38	SPARE	
J04-29	SPARE	

Table 2-8. I/O Channel Main-Storage Priority Order

Priority	Channel
Highest	Selector 1: Channel 4
	Integrated Disk Adapter: Channel 3
	Selector 2: Channel 6
	Multiplexer Channel: Channel 1
	Integrated Peripheral Channel: Channel 0
Lowest	Processor or I/O Status Tabler: Channel 7

SECTION 3

IPC AND PERIPHERALS

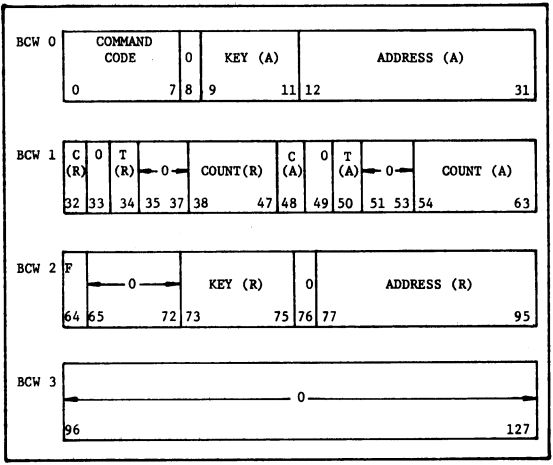


Figure 3-1. IPC Buffer Control Word Format

Table 3-1. IPC Buffer Control Word

Bit	Field	Description
0 - 7	Command Code	Contains a command which is accessed by the IPC after the Start I/O instruction. This command is transfered to the appropriate device control logic.
8		Unassigned, must be zero.
9 - 11	Key (A)	Active key field. This field contains the I/O storage protection key. This key is presented to main storage interface during all data transfer sequences. The IPC does not modify the key field during these sequences; if the IPC generates a key, it is equal to zero.
12-31	Address (A)	Active address field specifies the absolute main storage address to be accessed during a data transfer sequence. The field is updated by the IPC during each sequence. The IPC uses the least significant bit (bit 31) only for byte-oriented transfer sequences. For half-word transfer sequences, only bits 12-30 are required. Replace
32	C (R)	Replacement chaining bit.
33		Unassigned, must be zero.
34	T (R)	Replacement termination.
35 - 37		Unassigned, must be zero.
38 - 47	Count (R)	Replacement count field.

Table 3-1. IPC Buffer Control Word (continued)

Bit	Field	Description
48	C (A)	Active chaining bit. When set to one, a data chaining operation is specified and the contents of the replacement fields are moved into the active fields before continuing with data transfer sequences. This field is ignored if the communication attachment feature (F1524-00) is not provided.
49		Unassigned, must be zero.
50	T (A)	Active termination bit. When set to one, indicates data transfer is to be terminated (when chaining is not specified) or that field replacement routine is to be performed (of chaining is specified).
51 - 53		Unassigned, must be zero.
54 - 63	Count (A)	Active count field. This field specifies the number of bytes of data to be transferred during the sequence. This count is decremented after each data transfer operation. When the field count decrements to zero, the T-field is set to one.
64	F	Flag bit. When set to one, indicates that contents of replacement fields are valid for a replacement operation. This field is tested when the active T and C bits both are set to one. The F bit is only used when the communication attachment feature (F1624-00) is provided.

Table 3-1. IPC Buffer Control Word (continued)

Bit	Field	Description
65 - 72		Unassigned, must be zero.
73 - 75	Key (R)	Replacement key field.
76		Unassigned, must be zero.
77 - 95	Address (R)	Replacement address field
96 - 127		Unassigned, must be zero.

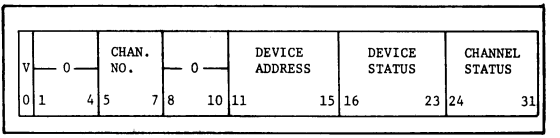


Figure 3-2. IPC IOSTIW Format

Table 3-2. IPC IOST Interrupt Word Description

Bit(s)	Designation	Description
0	V	IOST control bit. The IPC sets this bit to zero when storing the IOSTIW.
1-4		Not used.
5-7	Channel Number	The IPC channel number is zero.
8-10		Not used.
11-15	Device Address	

11	12	13	14	15	Device
0	0	0	0	0	Console (U-100)
0	0	0	0	1	0717/0719 Reader
0	0	0	1	0	0773/0778 Printer
0	0	0	1	1	0605 Punch
X	0	1	0	0	LA-0 (CA)
X	0	1	0	1	LA-6
X	0	1	1	0	LA-1
X	0	1	1	1	LA-7
X	1	0	0	0	LA-2
X	1	0	0	1	LA-8
X	1	0	1	0	LA-3
X	1	0	1	1	LA-9
X	1	1	0	0	LA-4
X	1	1	0	1	LA-10
X	1	1	1	0	LA-5
X	1	1	1	1	LA-11 (CA)

CA0 = X=0; CA1 = X=1

Table 3-2. IPC IOST Interrupt Word Description (cont)

Bit(s)	Designation	Description
16-23	Device Status	
24-31	Channel Status	

0	16	Attention
1	17	0
2	18	0
3	19	0
4	20	0
5	21	Device End
6	22	Unit Check
7	23	Unit Exception

0	24	0
1	25	0
2	26	0
3	27	Invalid Address
4	28	Channel Data Check
5	29	0
6	30	Channel Control Check
7	31	Buffer Terminate

Table 3-3. IPC SIO Condition Code

CC	Control State	Device State	Command Action	Int. Stored	IOSTIW Field
00	Available	Run	Accepted	Y (1)	Device (2)
01	Available	Stop	Rejected (3)	Y (1)	Device
10	Busy (4)	- - -	Rejected	N	- - -
11	Not Oper.	- - -	Rejected	N	- - -

(1) IOSTIW stored in the BCW on completion of command.

(2) Device status stored if no other errors occur.

(3) Sense of Diagnostic commands will not be rejected. (Condition Code will be 00_2.)

(4) IPC is considered Busy if pending status condition prevails.

Table 3-4. Translate Mode Conversion

Character Symbol	Punch Rows	USASCII Bit Position 0	1	2	3	4	5	6	7	EBCDIC Bit Position 0	1	2	3	4	5	6	7
SPACE	None	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
!	12-8-7	0	0	1	0	0	0	0	1	0	1	0	0	1	1	1	1
"	8-7	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1
#	8-3	0	0	1	0	0	0	1	1	0	1	1	1	1	1	0	1
$	11-8-3	0	0	1	0	0	1	0	0	0	1	0	1	1	1	0	1
%	0-8-4	0	0	1	0	0	1	0	1	0	1	1	0	1	1	1	0
&	12	0	0	1	0	0	1	1	0	0	1	0	1	0	0	0	0
'	8-5	0	0	1	0	0	1	1	1	0	1	1	1	1	1	1	0
(	12-8-5	0	0	1	0	1	0	0	0	0	1	0	0	1	1	0	1
)	11-8-5	0	0	1	0	1	0	0	1	0	1	0	1	1	1	0	1
*	11-8-4	0	0	1	0	1	0	1	0	0	1	0	1	1	1	0	0
+	12-8-6	0	0	1	0	1	0	1	1	0	1	0	0	0	1	1	0
,	0-8-3	0	0	1	0	1	1	0	0	0	1	1	0	1	0	1	1
-	11	0	0	1	0	1	1	0	1	0	1	1	0	0	0	0	0
.	12-8-3	0	0	1	0	1	1	1	0	0	1	0	0	1	0	1	1
/	0-1	0	0	1	0	1	1	1	1	0	1	1	0	0	0	0	1
0	0	0	0	1	1	0	0	0	0	1	1	1	1	0	0	0	0
1	1	0	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1
2	2	0	0	1	1	0	0	1	0	1	1	1	1	0	0	1	0
3	3	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1
4	4	0	0	1	1	0	1	0	0	1	1	1	1	0	1	0	0
5	5	0	0	1	1	0	1	0	1	1	1	1	1	0	1	0	1
6	6	0	0	1	1	0	1	1	0	1	1	1	1	0	1	1	0
7	7	0	0	1	1	0	1	1	1	1	1	1	1	0	1	1	1
8	8	0	0	1	1	1	0	0	0	1	1	1	1	1	0	0	0
9	9	0	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1
:	8-3	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	0
;	11-8-6	0	0	1	1	1	0	1	1	0	1	0	1	1	1	1	0
<	12-8-4	0	0	1	1	1	1	0	0	0	1	0	0	1	1	0	0
=	8-6	0	0	1	1	1	1	0	1	0	1	1	1	1	1	1	0
>	0-8-6	0	0	1	1	1	1	1	0	0	1	1	0	1	1	1	0
?	0-8-7	0	0	1	1	1	1	1	1	0	1	1	0	1	1	1	1
@	8-4	0	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
A	12-1	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1
B	12-2	0	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0
C	12-3	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1

Table 3-4. Translate Mode Conversion (cont)

Character Symbol	Punch Rows	USASCII Bit Position 0 1 2 3 4 5 6 7	EBCDIC Bit Position 0 1 2 3 4 5 6 7
D	12-4	0 1 0 0 0 1 0 0	1 1 0 0 0 1 0 0
E	12-5	0 1 0 0 0 1 0 1	1 1 0 0 0 1 0 1
F	12-6	0 1 0 0 0 1 1 0	1 1 0 0 0 1 1 0
G	12-7	0 1 0 0 0 1 1 1	1 1 0 0 0 1 1 1
H	12-8	0 1 0 0 1 0 0 0	1 1 0 0 1 0 0 0
I	12-9	0 1 0 0 1 0 0 1	1 1 0 0 1 0 0 1
J	11-1	0 1 0 0 1 0 1 0	1 1 0 1 0 0 0 1
K	11-2	0 1 0 0 1 0 1 1	1 1 0 1 0 0 1 0
L	11-3	0 1 0 0 1 1 0 0	1 1 0 1 0 0 1 1
M	11-4	0 1 0 0 1 1 0 1	1 1 0 1 0 1 0 0
N	11-5	0 1 0 0 1 1 1 0	1 1 0 1 0 1 0 1
O	11-6	0 1 0 0 1 1 1 1	1 1 0 1 0 1 1 0
P	11-7	0 1 0 1 0 0 0 0	1 1 0 1 0 1 1 1
Q	11-8	0 1 0 1 0 0 0 1	1 1 0 1 1 0 0 0
R	11-9	0 1 0 1 0 0 1 0	1 1 0 1 1 0 0 1
S	0-2	0 1 0 1 0 0 1 1	1 1 1 0 0 0 1 0
T	0-3	0 1 0 1 0 1 0 0	1 1 1 0 0 0 1 1
U	0-4	0 1 0 1 0 1 0 1	1 1 1 0 0 1 0 0
V	0-5	0 1 0 1 0 1 1 0	1 1 1 0 0 1 0 1
W	0-6	0 1 0 1 0 1 1 1	1 1 1 0 0 1 1 0
X	0-7	0 1 0 1 1 0 0 0	1 1 1 0 0 1 1 1
Y	0-8	0 1 0 1 1 0 0 1	1 1 1 0 1 0 0 0
Z	0-9	0 1 0 1 1 0 1 0	1 1 1 0 1 0 0 1
[	12-8-2	0 1 0 1 1 0 1 1	0 1 0 0 1 0 1 0
\	0-8-2	0 1 0 1 1 1 0 0	1 1 1 0 0 0 0 0
]	11-8-2	0 1 0 1 1 1 0 1	0 1 0 1 1 0 1 0
^	11-8-7	0 1 0 1 1 1 1 0	0 1 0 1 1 1 1 1
_	0-8-5	0 1 0 1 1 1 1 1	0 1 1 0 1 1 0 1
`	8-1	0 1 1 0 0 0 0 0	0 1 1 1 1 0 0 1
a	12-0-1	0 1 1 0 0 0 0 1	1 0 0 0 0 0 0 1
b	12-0-2	0 1 1 0 0 0 1 0	1 0 0 0 0 0 1 0
c	12-0-3	0 1 1 0 0 0 1 1	1 0 0 0 0 0 1 1
d	12-0-4	0 1 1 0 0 1 0 0	1 0 0 0 0 1 0 0
e	12-0-5	0 1 1 0 0 1 0 1	1 0 0 0 0 1 0 1
f	12-0-6	0 1 1 0 0 1 1 0	1 0 0 0 0 1 1 0
g	12-0-7	0 1 1 0 0 1 1 1	1 0 0 0 0 1 1 1

Table 3-4. Translate Mode Conversion (cont)

Character Symbol	Punch Rows	USASCII Bit Position 0 1 2 3 4 5 6 7	EBCDIC Bit Position 0 1 2 3 4 5 6 7
h	12-0-8	0 1 1 0 1 0 0 0	1 0 0 0 1 0 0 0
i	12-0-9	0 1 1 0 1 0 0 1	1 0 0 0 1 0 0 1
j	12-11-1	0 1 1 0 1 0 1 0	1 0 0 1 0 0 0 1
k	12-11-2	0 1 1 0 1 0 1 1	1 0 0 1 0 0 1 0
l	12-11-3	0 1 1 0 1 1 0 0	1 0 0 1 0 0 1 0
m	12-11-4	0 1 1 0 1 1 0 1	1 0 0 1 0 1 0 0
n	12-11-5	0 1 1 0 1 1 1 0	1 0 0 1 0 1 0 1
o	12-11-6	0 1 1 0 1 1 1 1	1 0 0 1 0 1 1 0
p	12-11-7	0 1 1 1 0 0 0 0	1 0 0 1 0 1 1 1
q	12-11-8	0 1 1 1 0 0 0 1	1 0 0 1 1 0 0 0
r	12-11-9	0 1 1 1 0 0 1 0	1 0 0 1 1 0 0 1
s	11-0-2	0 1 1 1 0 0 1 1	1 0 1 0 0 0 1 0
t	11-0-3	0 1 1 1 0 1 0 0	1 0 1 0 0 0 1 1
u	11-0-4	0 1 1 1 0 1 0 1	1 0 1 0 0 1 0 0
v	11-0-5	0 1 1 1 0 1 1 0	1 0 1 0 0 1 0 1
w	11-0-6	0 1 1 1 0 1 1 1	1 0 1 0 0 1 1 0
x	11-0-7	0 1 1 1 1 0 0 0	1 0 1 0 0 1 1 1
y	11-0-8	0 1 1 1 1 0 0 1	1 0 1 0 1 0 0 0
z	11-0-9	0 1 1 1 1 0 1 0	1 0 1 0 1 0 0 1
{	12-0	0 1 1 1 1 0 1 1	1 1 0 0 0 0 0 0
:	12-11	0 1 1 1 1 1 0 0	0 1 1 0 1 0 1 0
}	11-0	0 1 1 1 1 1 0 1	1 1 0 1 0 0 0 0
~	11-0-1	0 1 1 1 1 1 1 0	1 0 1 0 0 0 0 1
DEL	12-9-7	0 1 1 1 1 1 1 1	0 0 0 0 0 1 1 1

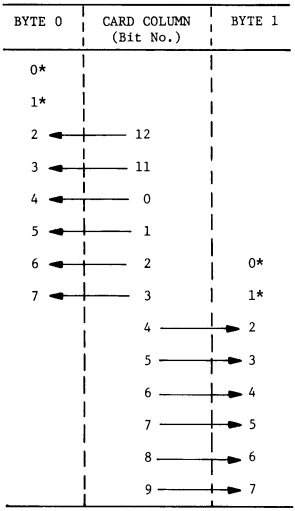
Table 3-5. 0717/0719 Card Reader Commands

Command \ Bit	0	1	2	3	4	5	6	7
Read	A	B	X	D	E	F	1	0
Sense	X	X	X	X	0	1	0	0

Note: X = Bit is ignored by the Reader Control.
A, B, D, E, F = Modifier bits.

Modifier Bit	Meaning
A=0	Normal read operation
A=1	Diagnostic use only
B=0	Normal read operation
B=1	Select read station 2 only, inhibit compare Error
D=X, E=0	Standard card, 80 column read
D=0, E=1	Short card, 51 column read
D=1, E=1	Short card, 66 column read
F=0	Read in Translate mode
F=1	Read in Image mode

Table 3-6. 0717/0719 Card Reader Image Mode Conversion



*Bits 0 and 1 of both image mode bytes are set to 0 by reader control.

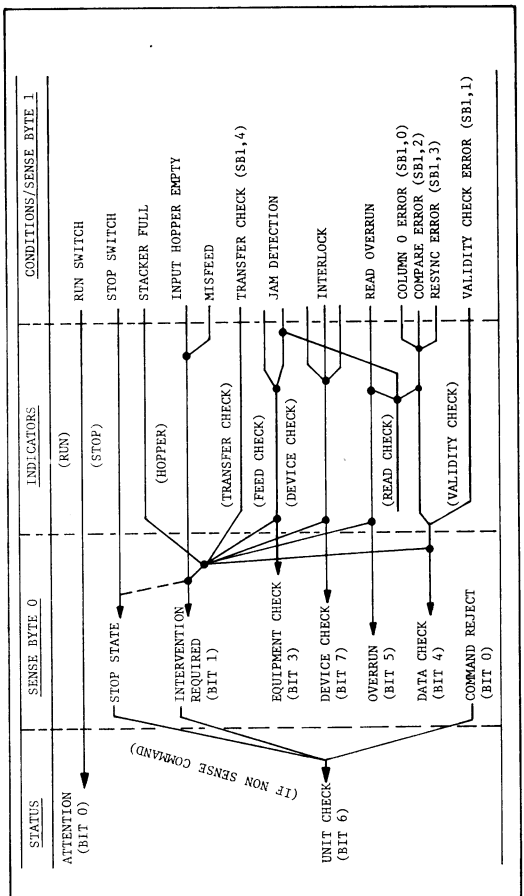


Figure 3-3. Summary of 0717/0719 Card Reader Status and Sense

Table 3-7. 0717/0719 Card Reader Status/Sense Bytes

	Status	Sense 0	Sense 1
Bit 0	Attention	Command Reject	Column 0 Error
Bit 1	-	Intervention Required	Validity Ck. Error
Bit 2	-	-	Compare Error
Bit 3	-	Equipment Check	Resync Error
Bit 4	-	Data Check	Transfer Check
Bit 5	Device End	Overrun	-
Bit 6	Unit Check	Stop State	Feature 51 Column
Bit 7	-	Device Check	Feature 66 Column

Table 3-8. 0605 Punch Commands

Bit / Command	0	1	2	3	4	5	6	7
Control	A	B	X	X	E	F	R	P
Sense	X	X	X	X	0	1	0	0

Note: X = Bit is ignored by the Punch Control.
A, B, E, F, R, P = Modifier bits.

Modifier Bit	Meaning
A=0	Normal punch/read operation
A=1	Diagnostic use only
B=0	Stop on error
B=1	Sort errors and remain in Run state
E=0	Normal punch operation
E=1	Select reject stacker
F=0	Punch and/or read in translate mode
F=1	Punch and/or read in Image mode
R=0, P=0	Invald code
R=1, P=0	Read operation
R=0, P=1	Punch operation
R=1, P=1	Punch and read operation

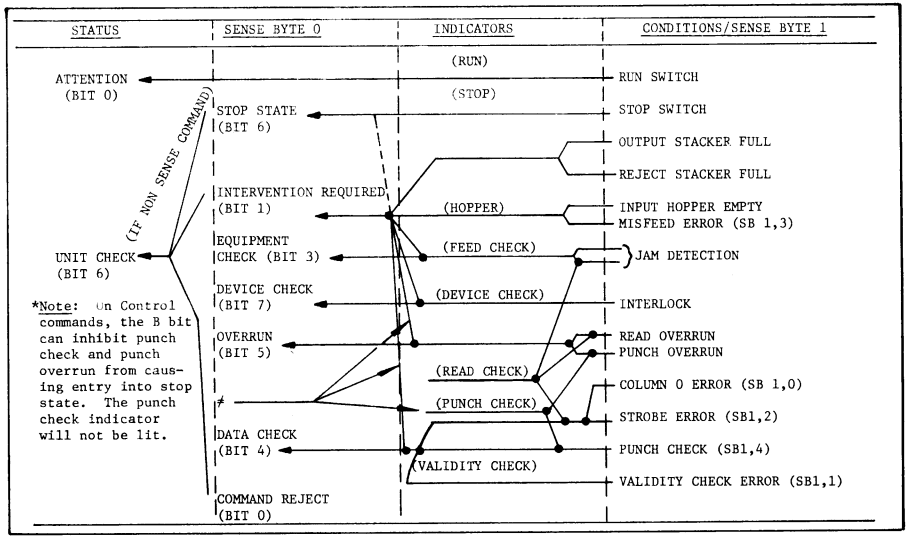


Figure 3-4. Summary of 0605 Punch Status and Sense

Table 3-9. 0605 Punch Status/Sense Bytes

	Status	Sense 0	Sense 1
Bit 0	Attention	Command Reject	Column 0 Error
Bit 1	-	Intervention Required	Validity Ck. Error
Bit 2	-	-	Strobe Error
Bit 3	-	Equipment Check	Misfeed Error
Bit 4	-	Data Check	Punch Check
Bit 5	Device End	Overrun	-
Bit 6	Unit Check	Stop State	Feature Read
Bit 7	-	Device Check	-

Table 3-10. 0773/0778 Printer Commands

Command \ Bit	0	1	2	3	4	5	6	7
Load V.F.B.	0	1	1	0	0	0	1	1
Load Code Buffer	1	1	1	1	1	0	1	1
Print Advance	A	C	D	E	F	0	0	1
Advance	A	C	D	E	F	1	1	1
*Load P.L.B.	1	1	1	0	0	0	1	1
*Read P.L.B.	X	X	X	0	0	0	1	0
*Read Load Code Buffer	X	X	X	0	1	0	1	0
*Read V.F.B.	A	X	X	1	0	0	1	0
*Diagnostic	X	X	X	X	X	1	0	0
Sense	X	X	X	X	0	1	0	0

Note: * = Diagnostic use only.

X = Bit is ignored by the Printer Control.

A, C, D, E, F = Modifier bits.

Modifier Bit	Meaning
(A=0) C, D, E, F	Line Advance (0~15 line)
(A=1) C	Ignored.
D, E, F	Skip code (0~7)
Read V.F.B.	The Read V.F.B. command (92_{16}) allows the readout of PLB and VFB areas. This is the only command that permits X bit readout of the PLB.

Table 3-11. 0773/0778 Printer Load Code Buffer Character Sequence (cont)

Load Code Buffer Address		Load Code Char. Seq.	48-Char. Business F1647-00	48-Char. Scientific F1647-01	63-Char. Set F1647-02	256 Expanded Char. Sets
Basic	Exp.	1. Character Sequence Code (Band ID) to ID Register 2. (Non-Printing Blank) to Space Register				
192	00	*3.	Z	Z	Z	
193	01	4.	Y	Y	Y	
194	02	5.	X	X	X	
195	03	6.	W	W	W	
196	04	7.	V	V	V	
197	05	8.	U	U	U	
198	06	9.	T	T	T	
199	07	10.	S	S	S	
200	08	11.	R	R	R	
201	09	12.	Q	Q	Q	
202	10	13.	P	P	P	
203	11	14.	O	O	O	
204	12	15.	N	N	N	
205	13	16.	M	M	M	
206	14	17.	L	L	L	
207	15	18.	K	K	K	
208	16	19.	J	J	J	
209	17	20.	I	I	I	
210	18	21.	H	H	H	
211	19	22.	G	G	G	
212	20	23.	F	F	F	
213	21	24.	E	E	E	
214	22	25.	D	D	D	
215	23	26.	C	C	C	
216	24	27.	B	B	B	
217	25	28.	A	A	A	
218	26	29.	9	9	9	
219	27	30.	8	8	8	
220	28	31.	7	7	7	
221	29	32.	6	6	6	
222	30	33.	5	5	5	
223	31	34.	4	4	4	
224	32	35.	3	3	3	
225	33	36.	2	2	2	
226	34	37.	1	1	1	
227	35	38.	0	0	0	
228	36	39.	-	-	-	
229	37	40.	/	/	/	
230	38	41.	@	.	@	
231	39	42.	#	=	#	
232	40	43.	$	$	$	
233	41	44.	,	,	,	
234	42	45.	+	+	+	
235	43	46.	'	)	'	
236	44	47.	*	*	*	
237	45	48.	%	(	%	
238	46	49.	&	&	&	
239	47	50.	----------	----------	.	
240	48	**51.	@	'	:	
241	49	**52.	*	=	[	
242	50	**53.	'	)	-	
243	51	**54.	%	(	;	
244	52	55.	N/A	N/A	?	
245	53	56.				SEQ LCB9
246	54	57.			¬	249 246
247	55	58.			▬	250 247
248	56	59.			¯	251 248
249	57	60.			'	252 249
250	58	61.			;	253 250
251	59	62.			≥	254 251
252	60	63.			)	255 252
253	61	64.			>	256 253
254	62	65.			<	257 254
255	63	66.			0	258 255

ANY SEQUENCE

Bit / ID	01234567
48 CHAR	SXXXX100
64 CHAR	SXXXX010
EXP CHAR	SXXXX001

S=Ø AN OVERRUN WILL SET A UNIT CHECK AND BLOCK FORM ADVANCE

S=1 INHIBITS OVERRUN ACTION NOTED ABOVE

*NOTE: First Character After Font Mark
**NOTE: Dualed Character Positions

2853

COMPANY CONFIDENTIAL

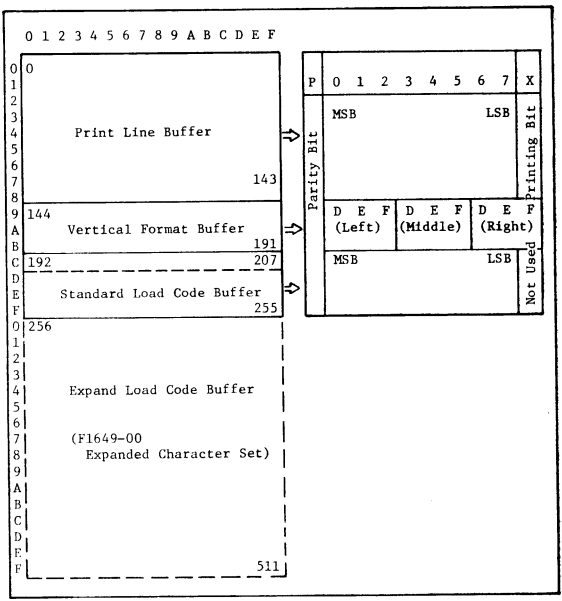


Figure 3-5. 0773/0778 Printer Buffer Locations

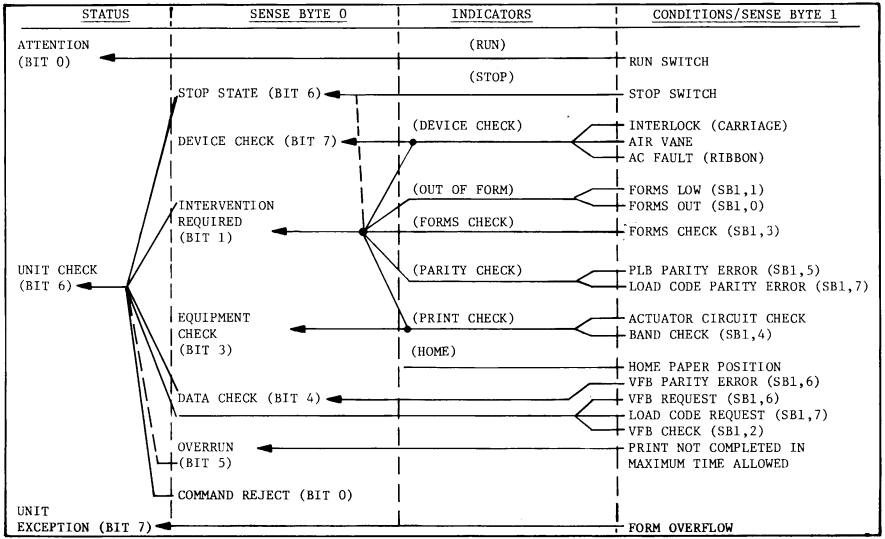


Figure 3-6. Summary of 0773/0778 Printer Status and Sense

Table 3-12. 0773/0778 Printer Status/Sense Bytes

	Status	Sense 0	Sense 1
Bit 0	Attention	Command Reject	Forms Out
Bit 1	-	Intervention Required	Forms Low
Bit 2	-	-	V.F.B. Check
Bit 3	-	Equipment Check	Forms Check
Bit 4	-	Data Check	Band Check
Bit 5	Device End	Overrun	P.L.B. Parity Error
Bit 6	Unit Check	Stop State	V.F.B Request or Parity Error
Bit 7	Unit Exception	Device Check	Load Code Request or Parity Error

Table 3-13. U100 Console Command

Command \ Bit	0	1	2	3	4	5	6	7
Read	A	X	X	X	X	F	1	0
Write	A	B	C	X	X	F	0	1
Sense	X	C	X	X	0	1	0	0

Note: X bit is ignored by the Console Control
A, B, C, F = Modifier bits

Table 3-14. U100 Modifier Bit Description

Modifier Bit	Meaning
A = 0	Normal read/write operation
A = 1	Diagnostic use only
B = 0	Lock Key Board at the completion of the Write sequence
B = 1	Unlock Key Board at the completion of the Write sequence
C = 0	Data transfer is to U100 only.
C = 1	Data transfer is to U100 and COP
F = 0	Read/write in Translate Mode. Translator is enabled.
F = 1	Read/write in ASCII Mode. Translator is bypassed.

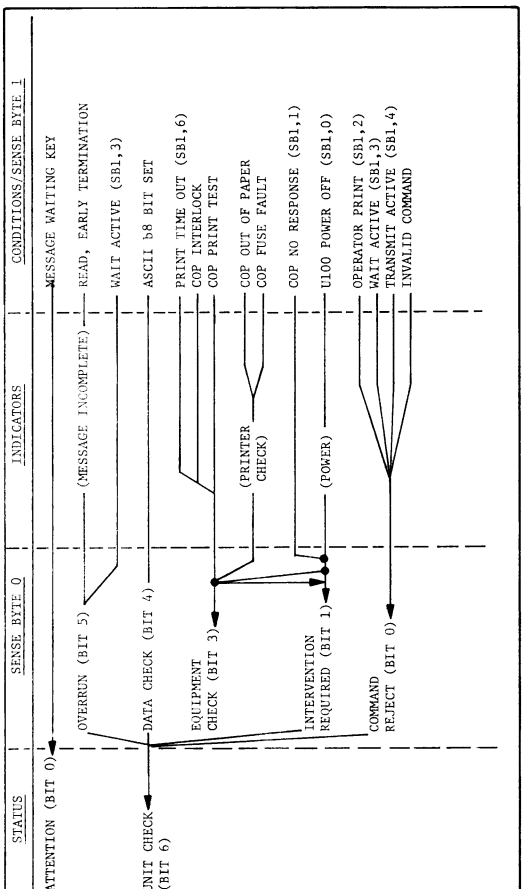


Figure 3-7. Summary of U100 Console Status and Sense

Table 3-15. U100 Console Sense and Status

	Status	Sense 0	Sense 1
Bit 0	Attention	Command Reject	U100 Power Off
Bit 1	-	Intervention Required	COP No Response
Bit 2	-	-	Operator Print
Bit 3	-	Equipment Check	Wait Active
Bit 4	-	Data Check	Transmit Active
Bit 5	Device End	Overrun	AI Feature
Bit 6	Unit Check	-	Print Time Out
Bit 7	-	-	-

Table 3-16. U100 Console Status Bits

Bit Position	Designation	Interpretation
0	Attention	Presented each time the operator depresses the Message Waiting Key on the U100.
1	N.A.	Set to zero by the control.
2	N.A.	Set to zero by the control.
3	N.A.	Set to zero by the control.
4	N.A.	Set to zero by the control.
5	Device End	Indicates the completion of a command.
6	Unit Check	Indicates at least one bit is set in Sense Byte 0.
7	N.A.	Set to zero by the control.

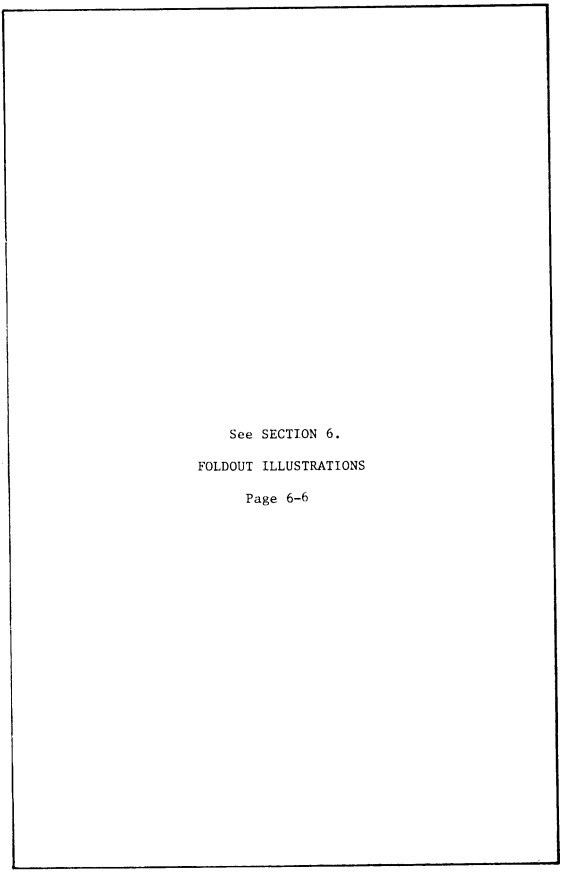


Figure 3-8. U100 Console Cursor Addressing For Screen Display

Table 3-17. EBCDIC to ASCII Translator

Upper / Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	00	10			20	26	2D						7B	7D	5C	30
1	01	11					2F		61	6A	7E		41	4A		31
2	02	12		16					62	6B	73		42	4B	53	32
3	03	13							63	6C	74		43	4C	54	33
4									64	6D	75		44	4D	55	34
5	09		0A						65	6E	76		45	4E	56	35
6		08	17						66	6F	77		46	4F	57	36
7	7F		1B	04					67	70	78		47	50	58	37
8		18							68	71	79		48	51	59	38
9		19						60	69	72			49	52	5A	39
A					5B	5D	7C	3A								
B	0B				2E	24	2C	23								
C	0C	1C		14	3C	2A	25	40								
D	0D	1D	05	15	28	29	5F	27								
E	0E	1E	06		2B	3B	3E	3D								
F	0F	1F	07	1A	21	5E	3F	22								

Table 3-18. ASCII to EBCDIC Translator

Upper / Lower	0	1	2	3	4	5	6	7
0	00	10	40	F0	7C	D7	79	97
1	01	11	4F	F1	C1	D8	81	98
2	02	12	7F	F2	C2	D9	82	99
3	03	13	7B	F3	C3	E3	83	A2
4	37	3C	5B	F4	C4	E3	84	A3
5	2D	3D	6C	F5	C5	E4	85	A4
6	2E	32	50	F6	C6	E5	86	A5
7	2F	26	7D	F7	C7	E6	87	A6
8	16	18	4D	F8	C8	E7	88	A7
9	05	19	5D	F9	C9	E8	89	A8
A	25	3F	5C	7A	D1	E9	91	A9
B	0B	27	4E	5E	D2	4A	92	C0
C	0C	1C	6B	4C	D3	E0	93	6A
D	0D	1D	60	7E	D4	5A	94	D0
E	0E	1E	4B	6E	D5	5F	95	A1
F	0F	1F	61	6F	D6	6D	96	07

Table 3-19. U100 Console Data Byte Format

IPC Bit Label	0	1	2	3	4	5	6	7
ASCII Bit Label	b8	b7	b6	b5	b4	b3	b2	b1
ASCII Bit Value	Y	Z	Z	Z	Z	Z	Z	Z

Y = Always Zero

Z = Seven bit ASCII code

Table 3-20. Character Set and Codes

CHARACTER SET		EBCDIC$_{16}$	ASCII$_8$	CHARACTER SET		EBCDIC$_{16}$	ASCII$_8$	CHARACTER SET		EBCDIC$_{16}$	ASCII$_8$	CHARACTER SET		EBCDIC$_{16}$	ASCII$_8$
1	!	4F	041	17	4	F1	261	33	A	C1	101	49	Q	D8	321
2	"	7F	042	18	2	F2	262	34	B	C2	102	50	R	D9	322
3	#	7B	243	19	3	F3	063	35	C	C3	303	51	S	E2	123
4	$	5B	044	20	4	F4	264	36	D	C4	104	52	T	E3	324
5	%	6C	245	21	5	F5	065	37	E	C5	305	53	U	E4	125
6	&	50	246	22	6	F6	066	38	F	C6	306	54	V	E5	126
7	'	7D	047	23	7	F7	267	39	G	C7	107	55	W	E6	327
8	(	4D	050	24	8	F8	270	40	H	C8	110	56	X	E7	330
9	)	5D	251	25	9	F9	071	41	I	C9	311	57	Y	E8	131
10	*	5C	252	26	:	7A	072	42	J	D1	312	58	Z	E9	132
11	+	4E	053	27	;	5E	273	43	K	D2	113	59	[	4A	333
12	,	6B	254	28	<	4C	074	44	L	D3	314	60	\	E0	134
13	-	60	055	29	=	7E	275	45	M	D4	115	61	]	5A	335
14	.	4B	056	30	>	6E	276	46	N	D5	116	62	^	5F	336
15	/	61	257	31	?	6F	077	47	O	D6	317	63	_	6D	137
16	0	F0	060	32	@	7C	300	48	P	D7	120	64	SP	40	240

Table 3-21. U100 Console Codes

Function	Code From Processor	Code To Processor	Hex Code ASCII	Hex Code EBCDIC
Erase Display	ESCM	-	1B, 4D	27, D4
Erase Unprotected Display	ESCa	-	1B, 61	27, 81
Erase to End of Line	ESCb	-	1B, 62	27, 82
Delete - In Line	ESCc	-	1B, 63	27, 83
Delete - In Display	ESCC	-	1B, 43	27, C3
Insert - In Line	ESCd	-	1B, 64	27, 84
Insert - In Display	ESCD	-	1B, 44	27, C4
Cursor to Home	ESCe	-	1B, 65	27, 85
Scan Up	ESCf	-	1B, 66	27, 86
Scan Left	ESCg	-	1B, 67	27, 87
Scan Right	ESCh	-	1B, 68	27, 88
Scan Down	ESCi	-	1B, 69	27, 89
Insert Line	ESCj	-	1B, 6A	27, 91
Delete Line	ESCk	-	1B, 6B	27, 92
Erase Field	ESCK	-	1B, 4B	27, D2
Tab	HT	HT	09	05
Tab Set	ESCHT	-	1B, 09	27, 05
Transmit Unprotected Display	DC1	-	11	11
Transmit Display	ESCDC1	-	1B, 11	27, 11
Print	DC2	-	12	12
Print Transparent	ESCDC2	-	1B, 12	27, 12
Line Feed	LF	LF	0A	25
Cursor Position	VT	VT	0B	0B
Form Feed	FF	FF	0C	0C
Carriage Return	CR	CR	0D	0D
Shift Out (Start Protected Field)	SO	-	0E	0E
Shift In (End Protected Field)	SI	SI	0F	0F
Lock Keyboard	DC4	-	14	3C
Skip Protected Data	-	SUB	1A	3F
Code Extention	ESC	ESC	1B	27
Start Blink Field	FS	FS	1C	1C
End Blink Field	GS	GS	1D	1D
Start of Entry (SOE)	RS	RS	1E	1E
Character Erase (Space)	SP	SP	20	40

Table 3-22. 8413 Diskette Subsystem Commands

Command	Mnemonic	Command Code (Hex)	Data Transfer Mode	Max. No. Of Bytes Transferred
Load Track & Sector	LTS	12/31	B	2
Read Index	RI	12	W	128
Read Index Deleted	RID	52	W	128
Write Index	WI	11	W	128
Write Index Deleted	WID	51	W	128
Read	R	Ø2	W+B	-
Read Deleted	RD	42	W+B	-
Write	W	Ø1	W+B	-
Write Deleted	WD	41	W+B	-
Diagnostic Read	DR	82-F2	W	-
Diagnostic Write	DW	81-F1	W	-
Sense	Sense	X4	B	6

B = Byte, W = Word, X = Don't Care

Table 3-23. 8413 FDC LED Indications For ILCS or IPL

Bit 2*	Bit 1*	Bit 0*	Indication	Functional Area (See Table 3-24)
0	0	0	LED Test Failed	Processor
0	0	1	ACC Load Failed	Processor
0	1	0	RAM 1's Failed	Processor (838)
0	1	1	RAM 0's Failed	Processor (838)
1	0	0	RAM Parity Error	Processor
1	0	1	Disk Reg. Load Failed	Disk
1	1	0	IPC File Load Failed	Interface
1	1	1	Diagnostics Complete	All Tests Passed

NOTE:

The "PROC CHK" LED is a hardware check to indicate an occurrence of one of two possible errors, either of which may require subsystem maintenance. The LED "On" means either, (1) a PROM Parity Error occurred, indicating possible firmware (PROM) malfunctions, or (2) the interval timer expired, indicating that the current command has taken too long (greater than 10 seconds) to execute. Malfunction may be due to mechanical disk problems or PROM failure.

*Refer to figure 3-9.

Table 3-24. 8413 FDC Subsystem Functional Areas

Functional Area	PC Assy #3625---*	PC Card Location*
Processor	841, 838, 839, 840, 833	07, 09, 11, 12, 13
Interface	835, 836, 837	03, 04, 05
Disk	842, 843, 844, 845, 837	15, 16, 17, 18, 05

*Refer to figure 3-10.
**841 refers to 07, 838 refers to 09, etc.

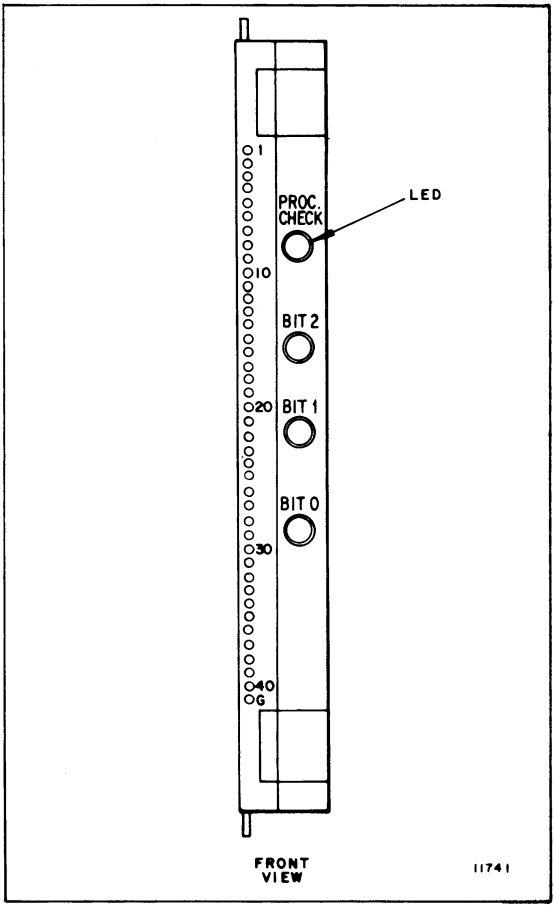
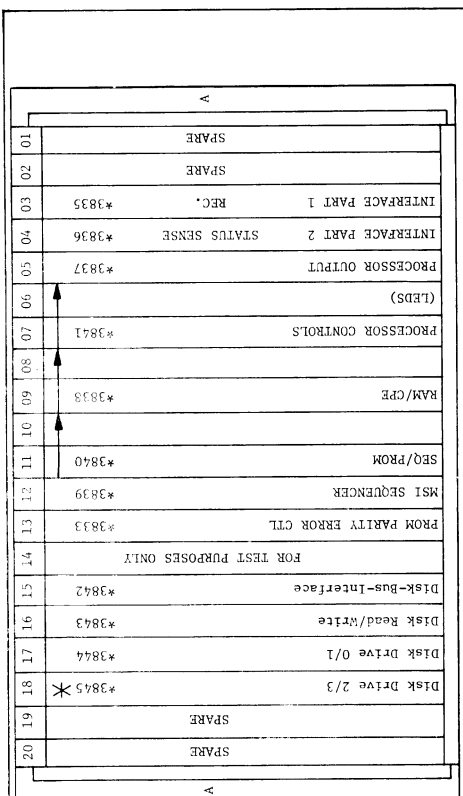
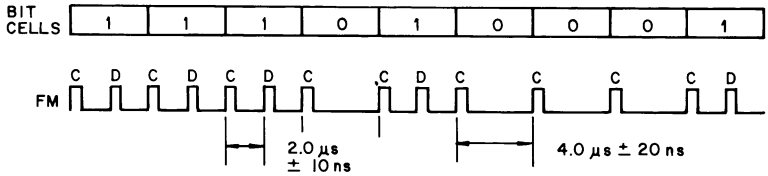


Figure 3-9. 8413 FDC Processor Control PC Board



NOTES:
1. * Reserved for feature F2653-00 & -01
2. ←→ Indicates two card spaces.
3. * Last four digits of logic page 3873----.

Figure 3-10. 8413 FDC PC Complement, Module 65



FM ENCODE

WRITE DATA BITS (D) AT THE CENTER OF THE BIT CELL.
WRITE CLOCK BITS (C) AT THE LEADING EDGE OF THE BIT CELL.

11333

Figure 3-11. 8413 Diskette FM Encoding

Table 3-25. 8413 Diskette Track Layout

Track	Description
ØØ	The index track. Its 26 sectors are used for system and data set label information.
Ø1-73	The actual data tracks where user information is recorded.
74	Not used.
75-76	Spare tracks that are used as data tracks when there are bad tracks in Ø1-73.

Table 3-26. 8413 Diskette Sector Layout
(Ref. Figures 3-12 and 3-13)

Sector	Description
Ø1, Ø2	8Ø blanks.
Ø3	Position 1 is reserved for a write test; 2-8Ø are blanks.
Ø4	8Ø blanks.
Ø5	Bad track information.
Ø6	8Ø blanks.
Ø7	Volume label information.
Ø8	The first data set label.
Ø9-26	Any additional data set labels.

Table 3-27. Sector 5 Bad Track Data (Ref. Figure 3-12)

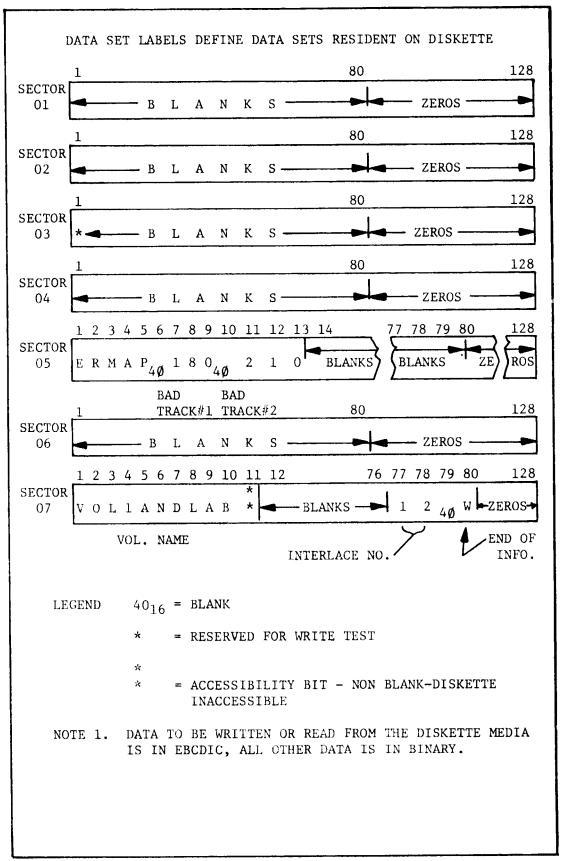
Bit Position	Description
1-5	ERMAP
6	Blank
7-8	The first bad track number
9	A zero
1Ø	Blank
11-12	The second bad track number
13	A zero
14-8Ø	Blanks

Table 3-28. Sector 7 Volume Label Data (Ref. Figure 3-12)

Bit Position	Description
1-4	VOL1
5-1Ø	The six character volume name
11	The accessibility bit - any non-blank character means this diskette is not accessible
12-76	Blanks
77-78	The sector sequence number
79	Blank
8Ø	A "W"

Table 3-29. Sectors 8-26 Track Data (Ref. Figure 3-13)

Bit Positions	Description
1-4	HDR1
5	Blank
6-13	An eight character data set name
14-22	Blanks
23-27	Record length
28	Blank
29-33	Beginning of extent (BOE) address
34	Blank
35-39	End of extent (EOE) address
4Ø	Blank
41	Bypass data set indicator
42	Accessibility bit
43	Write protect
44	Interchange type indicator
45	Multivolume indicator
46-47	Volume sequence number
48-53	Creation date
54-66	Blanks
67-72	Expiration date
73	Verify indicator
74	Blank
75-79	End of data (EOD) address
8Ø	Blank



LEGEND 40_{16} = BLANK

* = RESERVED FOR WRITE TEST

*
* = ACCESSIBILITY BIT - NON BLANK-DISKETTE INACCESSIBLE

NOTE 1. DATA TO BE WRITTEN OR READ FROM THE DISKETTE MEDIA IS IN EBCDIC, ALL OTHER DATA IS IN BINARY.

Figure 3-12. 8413 Diskette Data Set Label Format Index Track Ø (Sectors 01-07)

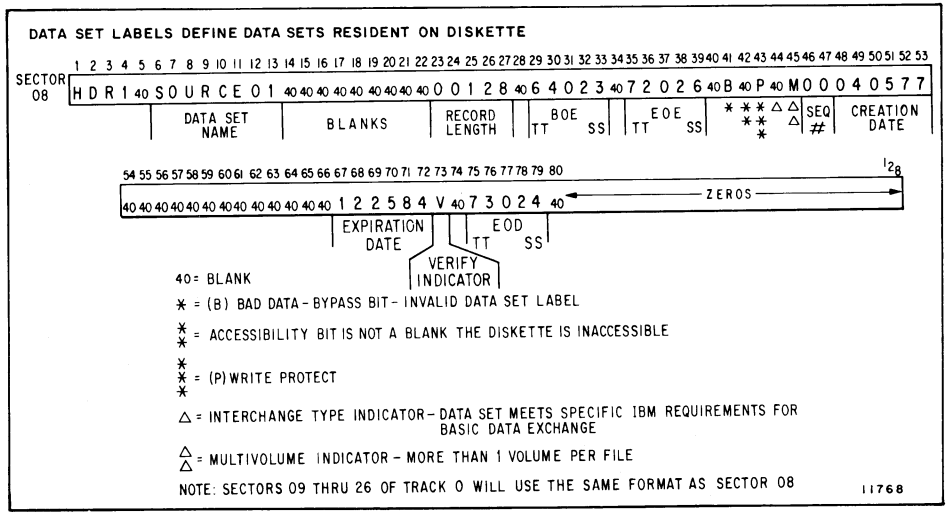

DATA SET LABELS DEFINE DATA SETS RESIDENT ON DISKETTE
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
SECTOR 08
HDR1 40 SOURCE 01 40 40 40 40 40 40 40 40 40 40 0 0 1 2 8 40 6 4 0 2 3 40 7 2 0 2 6 40 B 40 P 40 M 0 0 0 4 0 5 7 7
DATA SET NAME
BLANKS
RECORD LENGTH
BOE
TT
SS
EOE
TT
SS
SEQ #
CREATION DATE
54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
12 8
40 40 40 40 40 40 40 40 40 40 40 40 40 1 2 2 5 8 4 V 40 7 3 0 2 4 40
ZEROS
EXPIRATION DATE
EOD
TT
SS
VERIFY INDICATOR
40 = BLANK
* = (B) BAD DATA - BYPASS BIT - INVALID DATA SET LABEL
** = ACCESSIBILITY BIT IS NOT A BLANK THE DISKETTE IS INACCESSIBLE
*** = (P) WRITE PROTECT
△ = INTERCHANGE TYPE INDICATOR - DATA SET MEETS SPECIFIC IBM REQUIREMENTS FOR BASIC DATA EXCHANGE
△△ = MULTIVOLUME INDICATOR - MORE THAN 1 VOLUME PER FILE
NOTE: SECTORS 09 THRU 26 OF TRACK 0 WILL USE THE SAME FORMAT AS SECTOR 08
11768

Figure 3-13. 8413 Diskette Data Set Label Format Index Track 0 (Sectors 08-26)

Table 3-30. 8413 Diskette Sector Sequences

The numerical order of the sectors around a track can be specified during the diskette initialization procedure to be any one of 13 different arrangements. These sector sequences are tabulated in the following chart:

Selected Sequence Displayed in Pos. 77 and 78. Record 07, Track 00. Blank or 01	Physical Sequence of Records in a Track																								
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
	Record Numbers - Sector Address																									
02	1	3	5	7	9	11	13	15	17	19	21	23	25	2	4	6	8	10	12	14	16	18	20	22	24	26
03	1	4	7	10	13	16	19	22	25	2	5	8	11	14	17	20	23	26	3	6	9	12	15	18	21	24
04	1	5	9	13	17	21	25	2	6	10	14	18	22	26	3	7	11	15	19	23	4	8	12	16	20	24
05	1	6	11	16	21	26	2	7	12	17	22	3	8	13	18	23	4	9	14	19	24	5	10	15	20	25
06	1	7	13	19	25	2	8	14	20	26	3	9	15	21	4	10	16	22	5	11	17	23	6	12	16	24
07	1	8	15	22	2	19	1	23	3	10	17	24	4	11	19	25	5	12	19	26	6	13	20	7	14	21
08	1	9	17	25	2	10	18	26	3	11	19	4	12	20	5	13	21	5	14	22	7	15	23	8	16	24
09	1	10	19	2	11	20	3	12	21	4	13	22	6	14	23	6	15	24	7	16	25	8	17	26	9	18
10	1	11	21	2	12	22	3	13	23	4	14	24	5	15	25	6	16	26	7	17	8	18	9	19	10	29
11	1	12	23	2	13	24	3	14	25	4	15	26	5	16	6	17	7	18	8	19	9	29	10	21	11	22
12	1	13	25	2	14	26	3	15	4	16	5	17	6	18	7	19	8	20	9	21	10	22	11	23	12	24
13	1	14	2	15	3	16	4	17	5	18	6	19	7	20	8	21	9	22	10	23	11	24	12	25	13	26

11770

REVISION: HCB-2

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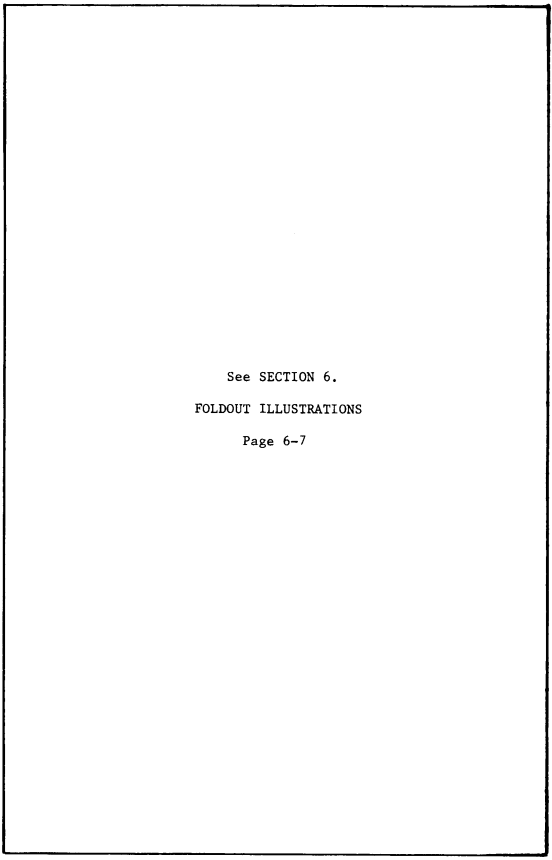
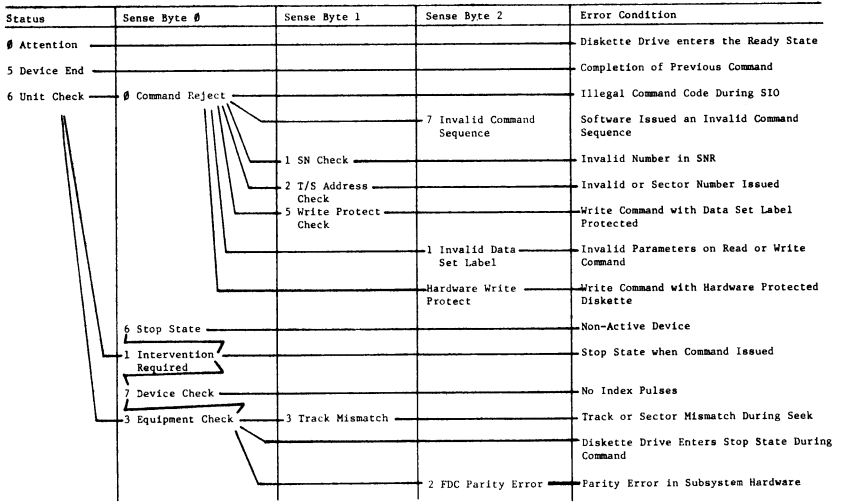


Figure 3-14. Diskette FM Track Format

Table 3-31. 8413 Diskette Status/Sense Error Conditions



REVISION: HCB-2

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Table 3-31. 8413 Diskette Status/Sense Error Conditions (cont)

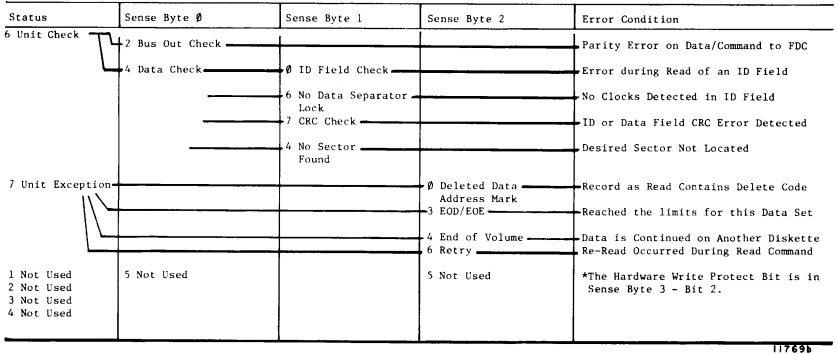
Status
Sense Byte Ø
Sense Byte 1
Sense Byte 2
Error Condition
6 Unit Check
2 Bus Out Check
Parity Error on Data/Command to FDC
4 Data Check
Ø ID Field Check
Error during Read of an ID Field
6 No Data Separator Lock
No Clocks Detected in ID Field
7 CRC Check
ID or Data Field CRC Error Detected
4 No Sector Found
Desired Sector Not Located
7 Unit Exception
Ø Deleted Data Address Mark
Record as Read Contains Delete Code
3 EOD/EOE
Reached the limits for this Data Set
4 End of Volume
Data is Continued on Another Diskette
6 Retry
Re-Read Occurred During Read Command
1 Not Used
2 Not Used
3 Not Used
4 Not Used
5 Not Used
5 Not Used
*The Hardware Write Protect Bit is in Sense Byte 3 - Bit 2.
11769b

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Table 3-32. 8413 Diskette Status/Sense Byte Summary

	Status Byte	Sense Byte Ø	Sense Byte 1	Sense Byte 2	Sense Byte 3	Sense Byte 4	Sense Byte 5
Bit Ø (MSB)	Attention	Command Reject	ID Field Check	Deleted Data AMD	Direct Access Mode	Not Used (Ø)	Not Used (Ø)
Bit 1	Not Used (Ø)	Inter-vention Required	SN Check	Invalid Data Set Label	Feature Installed	TAØ	Not Used (Ø)
Bit 2	Not Used (Ø)	Bus Out Check	Track/ Sector Address Check	FDC Parity Protect	Hardware Write	TA1	Not Used (Ø)
Bit 3	Not Used (Ø)	Equipment Check	Track Mismatch	EOD/EOE	SNRØ	TA2	SAØ
Bit 4	Not Used (Ø)	Data Check	No Sector Found	End of Volume	SNR1	TA3	SA1
Bit 5	Device End	Not Used (Ø)	Write Protect Check	Not Used (Ø)	SNR2	TA4	SA2
Bit 6	Unit Check	Stop State	No Data Separator Lock	Retry	SNR3	TA5	SA3
Bit 7 (LSB)	Unit Exception	Device Check	CRC Check	Invalid Command Sequence	SNR4	TA6	SA4

11771

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Table 3-33. 8413 Diskette Error Table

Condition Code (Binary	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
11	-	-	A	6,7	FDC is not operational due to: 1. Illegal Device Address during SIO. 2. Power-on diagnostic test in progress. 3. Power-on diagnostic test error exists. 4. Not present or device experienced a non-recovered control store parity error. 5. 8413 instruction time has elapsed.
10	-	-	A	8	A Busy condition is generated when the following conditions exist during the SIO: 1. A pending Channel Status condition exists in the IPC for any control. 2. A pending Device Status condition exists in the FDC for any diskette drive. 3. A command is issued to the FDC while it is in the process of executing a previous command for any diskette drive.

Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
01	02	1000 0000 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,2	Unit Check (UC) Status/Command Reject - the FDC rejected the command during SIO due to an illegal command code.
01	02	0010 0000 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,2,3	Unit Check (UC) Status/Bus Out Check - The FDC rejected the command during SIO due to a command parity error.
01	02	1100 0010 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,1,2	Unit Check (UC) Status/Command Reject/Stop/Intervention Required - the FDC rejected the non-diagnostic command during SIO due to the addressed drive being in the stop state or not installed.
-	80	-	-	0	Attention Status - FDC has made a transition from the Stop to the Run state.

REVISION: HCB-2

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Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	04	0000 0000 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	-	0	Device End (DE) Status - indicates normal FDC ending status with no error/unusual condition.
00	06	0001 0000 0000 0000 0010 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,2 10,3	DE/UE/FDC Parity Error/Equipment Check - a subsystem RAM parity error was detected on the executive of the previous command.
00	06	0010 0000 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,2 10,3	DE/UC Bus Out Check - a parity error was detected on a data transfer to the FDC during the previous LTS, WI, WID, W, WD, or DW command.
00	06	0101 0001 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,2,3	DE/UC/Intervention Required/Equipment Check/Device Check - no drive index pulses are detected while executing an RI, RID, R, RD, WI, WID, W, WD, or LTS command is being executed.

Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	06	1000 0000 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,11	DE/UC/Cmnd Rjct - a DW(E1) command was issued without an immediately proceding DW(F1) enabling command.
00	06	1000 0000 0000 0000 0000 0000 1XXN NNNN 0TTT TTTT 000S SSSS	A	6,11	DE/UC/Cmd Rjct/DAM - an RI, RID, WI, WID, LTS 21 w track ≠ 0, or LTS 21 w track = 0 but no sector number specified, was issued while FDC is in the Direct Access Mode.
00	06	1000 0000 0100 0000 0000 0000 0XXN NNNN 0TTT TTTT 000S SSSS	A	6,12,2	DE/UC/Cmd Rjct/SN Check - invalid number in the SNR (Ø or > 26) when RI, RID, WI, WID, R, RD, W, or WD command was issued while FDC is in the Data Set Mode.

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Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	06	1000 0000 0010 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,12,2	DE/UC/Cmnd Rjct/TS Address Check-invalid number issued to the TAR or SAR during an LTS command.
00	06	1000 0000 0000 0000 0100 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,13,2	DE/UC/Cmnd Rjct/Invalid Data Set Label-invalid data set label parameters when R, RD, W, or WD command was issued.
00	06	1000 0000 0000 0100 0000 0000 0XON NNNN 0TTT TTTT 000S SSSS	A	6,14,2	DE/UC/Cmnd Rjct/Write Protect Check-the data set label is write protected when a W or WD command was issued and the FDC is in the Data Set Mode.

Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	06	1000 0000 0000 0100 0000 0000 XX1N NNNN 0TTT TTTT 000S SSSS	A	6,5,2	DE/UC/Cmd Rjct/Write Protect Check/Hardware Write Protect - a W, WD, WI, or WID command was issued to a hardware write protected diskette.
00	07	0000 1000 1000 0001 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	B	15,3,6	DE/UC/UE/Retry/Data Check/ID Field Check/CRC Check - retry of an ID field error was not successful on the previous command.
00	07	0000 1000 0000 0001 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	B	15,16 3,6	DE/UC/UE/Retry/Data Check/CRC Check - retry of a data CRC error was not successful on the previous command.

REVISION: HCB-2

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Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	07	0000 1000 1000 0010 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	B	15,3,6	DE/UC/UE/Retry/Data Check/No Data Separator Lock/ID Field Check - retry of a no data separator lock error was not successful on the previous command.
00	07	0001 0000 0001 0000 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	B	15,3,6	DE/UC/UE/Retry/Equipment Check/Track Mismatch - retry of a Track Mismatch error was not successful on the previous command.
00	05	0000 0000 1000 0001 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	C	3,4	DE/UE/Retry/ID Field Check/CRC Check - a successful retry of an ID Field Check error occurred on the previous command.

Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	05	0000 0001 0000 0001 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	C	3,4	DE/UE/Retry/CRC Check - a successful retry of a data CRC error occurred on the previous command.
00	05	0000 0000 0001 0000 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	C	3,4	DE/UE/Retry/Track Mismatch - a successful retry of a Track Mismatch error occurred on the previous command.
00	05	0000 0000 1000 0010 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	C	3,4	DE/UE/Retry/No Data Separator Lock/ID Field Check - a successful retry of a no data separator lock error occurred on the previous command.

Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	05	0000 0000 0000 0000 1000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	D	0,9	DE/UE/Deleted AM - a deleted record was transferred on the previous RD or RID command.
00	05	0000 0000 0000 0000 0001 0000 0XXN NNNN 0TTT TTTT 000S SSSS	D	0,9	DE/UE/(EOD/EOE) - the EOD or EOE record was transferred on the previous R, RD(EOD) or W, WD(EOE) command.
00	05	0000 0000 0000 0000 0000 1000 XXXN NNNN 0TTT TTTT 000S SSSS	D	0,9	DE/UE/End of Vol. - the last record of this volume was transferred on the previous R, RD, W, or WD command and another volume is required to continue.

Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	05	0000 0000 0000 0000 1001 0000 0XXN NNNN 0TTT TTTT 000S SSSS	D	0,9	DE/UE/Deleted AM/(EOD/EOE) - the EOD record was transferred on the previous RD command and it was a deleted record.
00	05	0000 0000 0000 0000 1000 1000 XXXN NNNN 0TTT TTTT 000S SSSS	D	0,9	DE/UE/Deleted AM/End of Vol. - the last record of this volume was transferred on the previous RD command and it was a deleted record. Also, another volume is required to continue.
00	06	0001 0000 0000 0000 0010 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,2 10,3	DE/UC/FDC Parity Error/Equipment Check - a recovered control store (ROM) parity error has occurred during the execution of the previous command.

REVISION: HCR-2

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Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	06	0000 0000 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,3 17	DE/UC - a non-recovered control store (ROM) parity error has occurred during the execution of the previous command or the subsystem timer has elapsed.
01	02	0000 0000 0000 0000 0000 0000 XXXN NNNN 0TTT TTTT	A	6,3	UC - the FDC rejected the command during SIO because a non-recoverable ROM parity error exists in the subsystem or the subsystem timer has elapsed.
00	07	0000 1000 0000 1000 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	B	15,3, 6	DE/UC/UE/Retry/Data Check/No Sector Found - retry of a No Sector Found error was not successful on the previous command.

Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	05	0000 0000 0000 1000 0000 0010 XXXN NNNN 0TTT TTTT 000S SSSS	C	3,4	DE/UE/Retry/No Sector Found - a successful retry of a No Sector Found error occurred on the previous command.
00	06	0000 1000 0000 0001 0000 0000 XXXN NNNN 0TTT TTTT 000S SSSS	A	3,6,18	DE/UC/CRC Check/Data Check - a read check error occurred on the previous Write command.
00	07	0000 1000 0000 0001 0001 0000 0XXN NNNN 0TTT TTTT 000S SSSS	A	3,6,19	DE/UC/UE/CRC Check/(EOD-EOE)/Data Check - a read check error occurred on the EOE record on the previous Write command.

REVISION: HCB-2

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Table 3-33. 8413 Diskette Error Table (cont)

Condition Code (Binary)	Status Byte (Hex)	Sense Bytes (Binary) 0123 4567	Priority	Recovery Procedure Order (See Table 3-34)	Error or Unusual Condition
00	07	0000 1000 0000 0001 0000 1000 XXXN NNNN 0TTT TTTT 000S SSSS	A	3,6,19	DE/UC/UE/CRC Check/(End of Vol.)/Data Check - a read check error occurred on the last record of a continued data set on the previous Write command.
00	06	1000 0000 0000 0000 0000 0001 XXXN NNNN 0TTT TTTT 000S SSSS	A	6,11	DE/UC/Cmnd Rjct/Invalid Cmnd Seq. - read command issued when TAR and SAR are equal to or greater than EOD value.
00	06	1000 0000 0010 0000 0000 0001 0XXN NNNN 0TTT TTTT 000S SSSS	A	6,11	DE/UC/Cmnd Rjct/TS Address/Invalid Cmnd Seq. - LTS(21) with track value of 1-74 issued after power-up or door closure.

NOTES FOR TABLE 3-33:

CC - the two bit condition code returned to the processor during initial selection to indicate the condition of the subsystem.

DE - the Device End status bit

UC - the Unit Check status bit

UE - the Unit Exception status bit

NNNNN - the five bit binary value in the addressed Sector Number Register (SNR0 - SNR4).

TTTTTTT - the seven bit binary value in the addressed Track Address Register (TA0 - TA6).

SSSSS - the five bit binary value in the addressed Sector Address Register (SA0 - SA4).

FDC - the Flexible Diskette Controller

X - don't care condition of the indicated sense bits.

Table 3-34. 8413 Diskette Recovery Procedure

No.	Recovery Procedure
0	No operator recovery procedure is necessary. There are no problems with the Diskette Control.
1	The operator should place the Diskette Control in the Run state by properly installing a diskette and closing the door of the drive.
2	After verifying that the command code is correct, the software should reissue the command which received Unit Check status.
3	The condition should be entered by software into the error log.
4	The software should continue by issuing the next command.
5	The operator should remove the current diskette and install a diskette that is not hardware write protected.
6	The software should display a message indicating the error.
7	The software/operator should: a. Software should verify that the device address is valid. b. Operator should verify that the addressed drive is installed. c. Operator should activate the System Reset switch. d. Software should reissue the command. e. If the error remains after three retries of the above procedure, operator should notify C.E.D.
8	Reissue the command when ending status is received.
9	The Sense bits present informational data as to the reason for the Unit Exception status.
10	Repeat Procedure 2 up to three times, if the error persists, notify C.E.D.
11	Software should issue the correct command or correct command sequence.
12	Software should correct error by issuing a valid LTS command.

Table 3-34. 8413 Diskette Recovery Procedure (cont)

No.	Recovery Procedure
13	Software should: a. Verify that the SNR value is in the range of 8 through 26. b. Read the Data Set Label. c. Determine the invalid parameter and correct it. d. Rewrite the valid Data Set Label.
14	Software should: a. Read the Data Set Label. b. Eliminate the write protect bit from the label. c. Rewrite the unprotected Data Set Label.
15	Software should: a. Issue a Sense command to determine the starting track and sector address of the previous command. b. Issue a LTS 21 command with the above track and sector values. c. Reissue the initial command that received Unit Check Status. d. If, after retrying up to three (3) times, the retry is not successful, display a message that the data is not recoverable. e. At this point, do one of the following - 1. Try the diskette on another drive. 2. Recover the data offline.

Table 3-34. 8413 Diskette Recovery Procedure (cont)

No.	Recovery Procedure
16	Software should: a. Issue a Sense command to determine the starting track and sector address of the previous command. b. Issue a LTS(21) command with the above track and sector values. c. Re-issue the initial command that received Unit Check status. d. Retry a, b, and c up to three times. e. If retries are not successful, issue a Diagnostic Read (82) to record buffer zero. f. Display the data to allow visual inspection and possible manual correction. g. Issue a Sense command to obtain the TAR and SAR values of the error sector. h. Increment the TAR, SAR values. i. Issue a LTS command with these new TAR and SAR values. j. Continue.
17	Software should reissue the command up to three times. If the error persists, operator should notify C.E.D.
18	Software should: a. Issue a Sense command to determine the starting track and sector address of the previous command. b. Issue an LTS(21) command with the above track and sector values. c. Re-issue the initial command that received Unit Check status. d. If, after retrying up to twelve (12) times, the retry is not successful, display a message that the data cannot be written. e. At this point, do one of the following: 1. LTS beyond the defective sector and continue from there. 2. Try to write on another drive.

Table 3-34. 8413 Diskette Recovery Procedure (cont)

No.	Recovery Procedure
19	Follow Procedure No. 18 except that it will not be possible to LTS beyond the defective sector in order to continue.

SECTION 4

IDA AND PERIPHERALS

Table 4-1. IDA Commands and Codes

BIT / COMMAND	0	1	2	3	4	5	6	7	DECODE
FORMAT* WRITE	0	0	0	0	0	0	0	1	01
WRITE* DATA	0	0	0	0	0	1	0	1	05
SEARCH/READ EQUAL*	0	0	0	0	1	0	0	1	09
SEARCH/READ* HI OR EQUAL	0	0	0	0	1	1	0	1	0D
READ* ID	0	0	0	0	1	1	1	0	0E
DIAGNOSTIC	0	0	0	0	0	1	1	0	06
READ DATA*	0	0	0	0	0	0	1	0	02
SEEK	0	0	0	0	1	0	0	0	08
SENSE	0	0	0	0	0	1	0	0	04
ECC DIAGNOSTIC	0	0	0	0	0	1	1	1	07
ECC SENSE	0	0	0	0	0	0	1	1	03

*Includes "IMPLIED" SEEK.

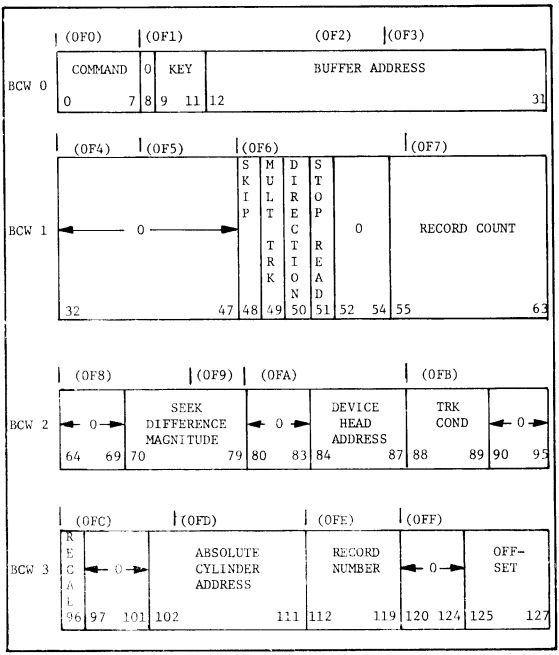

Figure 4-1. IDA Buffer Control Words

Table 4-2. IDA Buffer Control Word

Bit	Field	Description
0 - 7	Command Code	Contains a command which is accessed by the IDA after a Start I/O instruction.
8		Unassigned, must be zero.
9 - 11	Key	This field contains the I/O storage protection key. This key as presented to the main storage interface during data transfer operations.
12 - 31	Buffer Address	This field specifies the absolute main storage address to be accessed during the next data transfer sequence. This field is updated by the channel during each sequence.
32 - 47		Unassigned, must be zero.
48	Skip Sentinel	When set during a Search Read command, specifies that search begins at index. When set during a Read Data command, specifies that data cannot be transferred to main storage.
49	Multitrack Sentinel	When set during a Search Read command, specifies that search is limited to a cylinder boundary.
50	Direction Sentinel	When set, specifies disk file accessor movement is in direction of decreasing cylinder numbers. Has no meaning if Seek Difference Magnitude is zero or if Recalibrate bit is set.
51	Stop Read	When set, terminates the Read command on a record causing an error.
51 - 54		Unassigned, must be zero.
55 - 63	Record Count	This field indicates the number of bytes or records that are to be processed. Whether the count is in bytes or records is dependent upon the type of command being executed.
64 - 69		Unassigned, must be zero.
70 - 79	Seek Difference Magnitude	During a seek operation this field specifies the difference between the present accessor position and the desired location.

Table 4-2. IDA Buffer Control Word (cont)

Bit	Field	Description
80 - 83		Unassigned, must be zero.
84 - 87	Device Head Address	This field specifies the device head address for the current operation.
88 - 89	Track Condition	Indicates track condition for current operation. ØØ indicates normal track, other codes indicate defective track.
90 - 95		Unassigned, must be zero.
96	Recalibrate	When set, specifies the accessor is to move to cylinder zero.
97 -101		Unassigned, must be zero.
102-111	Absolute Cylinder Address	This field indicates the cylinder address.
112-119	Record Number	This field specifies the number of the record applicable to the present operation.
120-124		Unassigned, must be zero.
125-127	Offset	These bits specify the offset magnitude applicable to the device in use. 125 - Ø = Offset not used. 1 = Offset is used 126 - Distance Ø = 350 µ in. 1 = 700 µ in. 127 - Direction Ø = Positive 1 = Negative

Table 4-3. IDA Command Repertoire and Required BCW Field

BCW Field \ Command	Format Write	Write Data	Search RD/EQ	Search RD/Hi-EQ	Read ID	Read Data	Seek	Sense	ECC Sense	Diagnostic	ECC Diagnostic
	01	05	09	0D	0E	02	08	04	03	06	07
Command	•	•	•	•	•	•	•	•	•	•	•
Key	•	•	•	•	•	•		•	•	•	•
Address	•	•	•	•	•	•		•	•	•	•
Skip			•	•		•					
Multi-track			•	•							
Direction	•	•	•	•	•	•	•				
Record Count	•	•	•	•		•				•	•
Seek Dif. Mag.	•	•	•	•	•	•	•				
Head Address	•	•	•	•	•	•	•				
Track Condition	•	•	•	•		•					
Recalibrate	•	•	•	•	•	•	•				
Abs. Cyl. Address	•	•	•	•		•					
Record Number	•	•				•					
Programmed Offset			•	•	•	•	•				

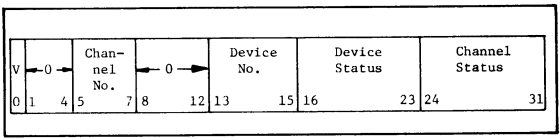

Figure 4-2. IDA IOST Interrupt Word

Table 4-4. IDA IOST Interrupt Word

Bit	Field	Description
0	V	The IDA sets this bit to zero when storing an interrupt word.
1-4	Channel No.	The IDA channel number is three.
8-12		Unassigned, must be zero.
13-15	Device No.	A binary code indicating the device associated with this entry.
16-23	Device Status	

0	16	Attention
1	17	0
2	18	0
3	19	Busy
4	20	Channel End
5	21	Device End
6	22	Unit Check
7	23	Unit Exception

Table 4-4. IDA IOST Interrupt Word

Bit	Field	Description		
24-31	Channel Status	0	24	0
		1	25	0
		2	26	0
		3	27	Invalid Address
		4	28	Channel Data Check
		5	29	0
		6	30	Channel Control Check
		7	31	0

Table 4-5. IDA Condition Codes

Condition Code	IDA State	Device State	Command Action	Interrupt Word Stored	Applicable Status Field In IOSTIW
00	Available	Run	Accepted	Yes (1)	Device (2)
01	Available	Busy	Reject (3)	Yes	Device
01	Available	Stop	Reject (3)	Yes	Device
10 (4)	Busy	-	Reject	No	-

(1) IOSTIW stored in the BCSW on completion of command.

(2) Device status stored, if no other errors occur (e.g. Channel Status).

(3) Sense of Diagnostic commands will not be rejected. (Condition Code will be 00_2.)

(4) Adapter is considered busy if pending status condition prevails.

Table 4-6. IDA Tag and File Bus

File Bus	Tag 0	Tag 1	Tag 2
FBU 0	Write Gate	Accessor Direction	Dif. Mag. 128
FBU 1	Read Gate	Dif. Mag. 512	Dif. Mag. 64
FBU 2	Seek Start	Dif. Mag. 256	Dif. Mag. 32
FBU 3	Offset Magnitude		Dif. Mag. 16
FBU 4	Offset Direction		Dif. Mag. 8
FBU 5	Head Select	Head Adr. 4	Dif. Mag. 4
FBU 6	Restore to 00	Head Adr. 2	Dif. Mag. 2
FBU 7	Offset	Head Adr. 1	Dif. Mag. 1

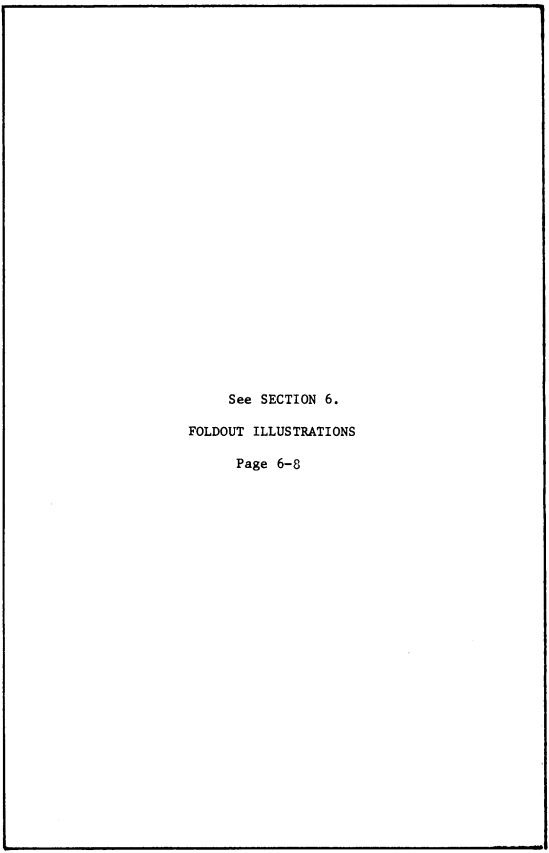

Figure 4-3. Summary of Status Bits, Sense Bits, and Error Conditions (IDA)

Table 4-7. IDA Sense Bytes

Bit No.	Sense Byte				
	Byte Ø	Byte 1	Byte 2	Byte 3	Byte 4
Bit Ø	Command Reject *	ID Field Check	Seek Incomplete *		
Bit 1	Inter-vention Required	Track Overrun	Comparison Parity Check		
Bit 2	Output Parity Check *	Cylinder End	Head/ Cylinder Miscompare		
Bit 3	Equipment* Check	8418 High Density	Record Number Miscompare		
Bit 4	Data Check	No Record Found	Flag Byte Miscompare		
Bit 5	Overrun	File Protect *	Unselected* Status	Head Number	Record Number
Bit 6	Stop State *	SYNC Region Error	ECC Check		
Bit 7	Device Check *	Data Field Check	No Clocks		

*These Sense Bits can be received after the Diagnostic has been executed.

Table 4-8. Summary of Sense Bits Possible For Each Command

Sense Bits			Format Write	Write Data	Read Data	Search Read	Read ID	Seek	Diagnostic
Command Reject	0	SB 0	•	•	•	•	•	•	•
Intervention Required	1		•	•	•	•	•	•	
Output Parity Check	2		•	•	•	•	•		•
Equipment Check	3		•	•	•	•	•	•	•
Data Check	4			•	•	•	•		
Overrun	5			•	•	•	•		
Stop State	6		•	•	•	•	•	•	•
Device Check	7		•	•	•	•	•	•	•
ID Field Check	0	SB 1		•	•	•	•		
Track Overrun	1		•	•	•	•	•		
Cylinder End	2			•	•	•			
	3								
No Record Found	4			•	•	•	•		
File Protect	5		•	•	•	•	•	•	•
Sync Region Error	6			•	•	•	•		
Data Field Check	7				•	•			
Seek Incomplete	0	SB 2	•	•	•	•	•	•	•
Comparison Parity Check	1			•	•	•	•		
Head/Cylinder Miscomp	2			•	•	•			
Record Number Miscomp	3			•	•	•			
Flag Byte Miscomp	4			•	•	•			
Unselected Status	5		•	•	•	•	•	•	•
ECC Check	6			•	•	•			
No Clocks	7		•	•	•	•	•		

COMPANY CONFIDENTIAL

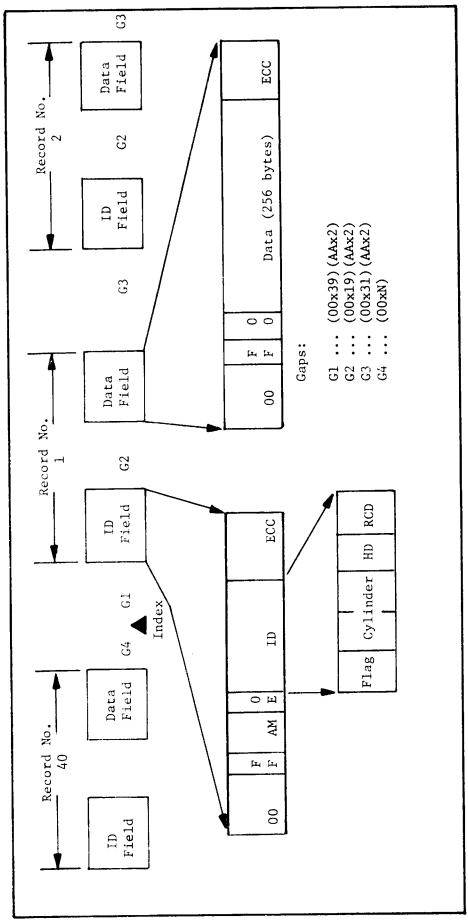

Figure 4-4. 8416 and 8418 Disk Track Format (1)

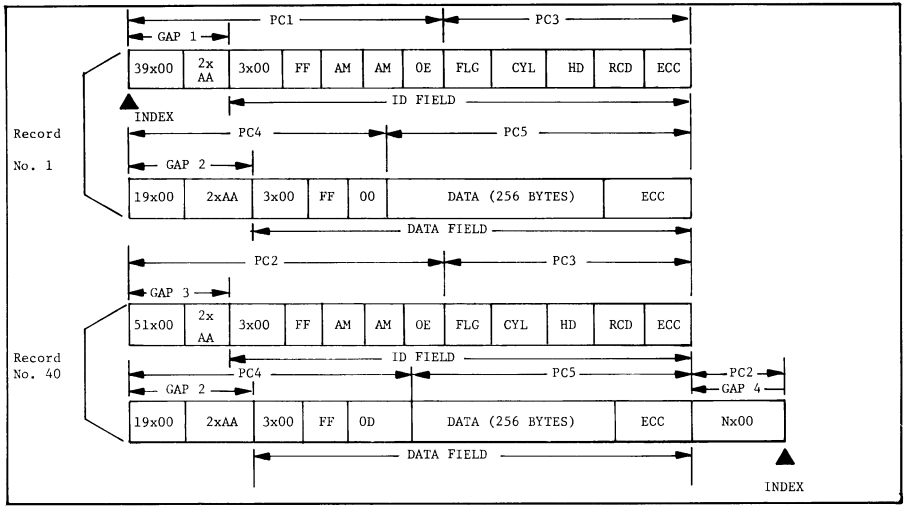

Figure 4-5. 8416 and 8418 Disk Track Format (2)

Table 4-9. Write Current Amplitude Per Cylinder Number

Cylinder Number	Write Current Amplitude (mil-amp)
000-063	79.5
064-127	86.5
128-191	83.0
192-255	79.75
256-319	76.5
320-383	73.25
384-410	70.0

Table 4-10. Unsafe Display LED's

Indicator	PWA Location
PLO Unsafe	A06
Heads Unsafe	B06
Pack Speed Unsafe	B12
Velocity Unsafe	B16
DC Write Unsafe	B16
AC Write Unsafe	B16
Read/Write Ready Unsafe	B16
AC Unsafe	B16

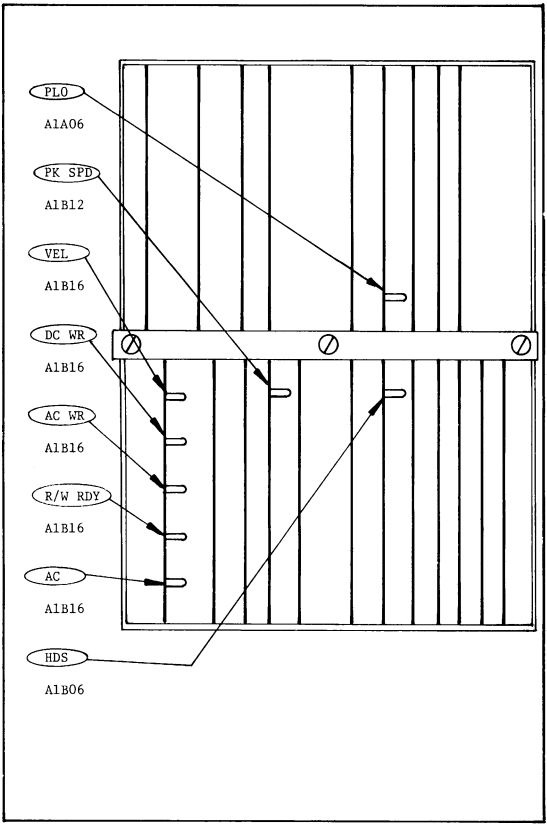

Figure 4-6. 8416 Electronic Gate Unsafe LED Indicators

8418 Unsafe CE Latch Outputs

Pin	
55	+ Power Unsafe
57	+ Write/Offset Unsafe
58	+ DC Write Unsafe
59	+ PGB Detect
60	+ PLO
62	+ Ac Write
64	+ Velocity
65	+ Pack Speed
66	+ Write Ready

SECTION 5

SELECTOR AND MULTIPLEXER CHANNELS

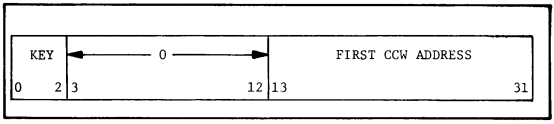

Figure 5-1. CAW Format (Selector Channel)

Table 5-1. CAW Field Description (Selector Channel)

Field	Bits	Meaning
Key	0-2	I/O Storage Protection Key that the channel will use for all storage accesses for data and CCW's related to the I/O operation initiated by this SIO instruction.
	3-12	Unassigned, must be zero.
First CCW Address	13-31	Specifies the address of the double word in storage which contains the first CCW.

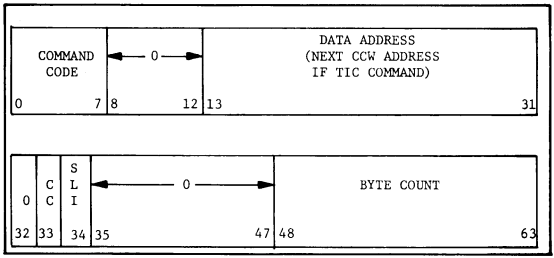

Figure 5-2. CCW Format (Selector Channel)

Table 5-2. CCW Field Description (Selector Channel)

Field	Bits	Meaning
Command Code	0-7	Specifies the operation to be performed by the device and channel.
	8-12	Unassigned, must be zeros.
Data Address	13-31	Contains the address of the location in storage into or from which the first byte of data will be transferred.
	32	Unassigned, must be zero.
CC	33	Chain Command flag.
SLI	34	Suppress Length Indication Flag.
	35-47	Unassigned, must be zeros.
Byte Count	48-63	The Byte Count is transferred to the channel and becomes the "Internal Byte Count". This count is decremented by one. So the Byte Count in the CCW is not altered.

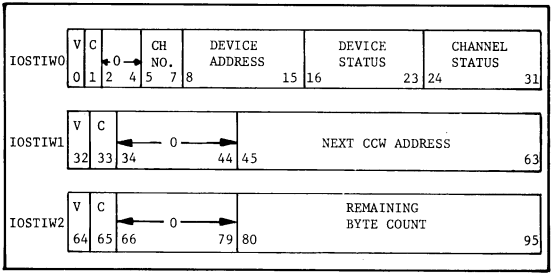

Figure 5-3. Selector Channel IOSTIW Format

Table 5-3. Selector Channel IOSTIW Field Description

Field	Bits	Meaning
V	0, 32, 64	Validation bit. Set to zero by selector channel.
C		Continuation bit.
	1	Always set to 1.
	33	Always set to 1.
	65	Always set to 0.
CH.NO.	5 - 7	Designates the channel number. Selector Ch. No. 1 - 100 (CH4) Selector Ch. No. 2 - 110 (CH6)
Device Address	8 - 15	Refer Table 5-6.
Device Status	16 - 23	Contains one byte of status generated by the subsystem. This field is always zero if only channel status is presented.
	16	Attention
	17	Status Modifier
	18	Control Unit End
	19	Busy
	20	Channel End
	21	Device End
	22	Unit Check
	23	Unit Exception

Table 5-3. Selector Channel IOSTIW Field Description (cont)

Field	Bits	Meaning
Channel Status	24 - 31	Contains a byte of status information generated by the channel.
	24	Set to 0 by the channel
	25	Incorrect length
	26	Program check
	27	Invalid Address
	28	Channel Data Check
	29	Interface Control Check
	30	Channel Control Check
	31	Set to 0 by the channel
Next CCW Address	45 - 63	The value of the next CCW address that was present in the internal channel hardware at the time the status word was written.
Remaining Byte Count	80 - 95	The value of the Byte Count that was present in the internal channel hardware at the time the status word was written.

Table 5-4. Channel Status Byte (Selector Channel)

Name	Meaning
Incorrect Length	1. Channel Byte Count ≠ Data Length
	2. On a Control Command Command chaining is specified or Separate Channel End and Device End status presentations are made.
Program Check	1. (CAW) CCW address not on double Word Boundary.
	2. (CCW) If TIC Command, CCW address not on double Word Boundary. First CCW contains TIC. Two consecutive TIC's
Invalid Address	1. (CAW) Address Exception or Protection (CCW) Exception
Channel Data Check	1. (CAW) Storage Parity Check (CCW)
	2. Bus in Parity Error.

Table 5-4. Channel Status Byte (Selector Channel)

Name	Meaning
Interface Control Check	1. Device Address or Status Byte Par. Error.
	2. Device Address non-match.
	3. Two in bound controls active simultaneously.
	4. A signal from a device occurred at the wrong time or was active or inactive for an accessive duration.
	5. During any ISS associated with command chaining, the device appeared non-operational or immediately Busy.
Channel Control Check	1. (CAW) Address Exception. (CCW) Address/Protection Exception.
	2. (CAW) Storage Read Check, Address Check. (CCW) Read Bus Check.

Table 5-5. Command Codes (Selector Channel)

Command Code Bits								Command
0	1	2	3	4	5	6	7	
M	M	M	M	1	0	0	0	TIC
M	M	M	M	0	1	0	0	Sense
M	M	M	M	M	M	0	1	Write
M	M	M	M	M	M	1	0	Read
M	M	M	M	1	1	0	0	Read Backward
M	M	M	M	M	M	1	1	Control
M	M	M	M	0	0	0	0	Test

Note: M bits are not interpreted by the channel.

Table 5-6. Device Addresses (Selector Channel)

Device Address Bits								Meaning
0	1	2	3	4	5	6	7	
1	X	X	X	X	X	X	X	Diagnostic Use
0	C	C	C	D	D	D	D	Normal format
								Address of one of 8 control units.
								Device number of one of 16 devices.

	SEL 1	SEL 2
DISK SUBSYSTEM T-8430	40X	N.A.
DISK SUBSYSTEM T-8411	41X	61X
UNISERVO 12/16 TAPE T-5017	43X	63X
DISK SUBSYSTEM T-8411/8414	44X	64X
DIAGNOSTIC CHANNEL (CUS TESTER)	480	680

Table 5-7. SIO Condition Codes (Selector Channel)

Condition Code	State			Command Action	IOSTIW Stored	Applicable Status Field in IOSTIW	Initial Selection Sequence (SU00039)
	Channel	Subchannel	Subsystem				
00	A	A	A	Accepted	Yes	Device	Yes
01	A	A	P	Rejected	Yes	Device	Yes
10	P	P	X	Rejected	Yes	Device and/or Channel	No
	W	W	X	Rejected	No	-	No
	A	A	W	Rejected	No	-	Attempted (Immediate BUSY)
11	N	X	X	Rejected	No	-	No
	X	X	N	Rejected	No	-	Attempted

Notes: A = Available; P = Status Pending; W = Working; N = Non-Operational; X = Any State.

Table 5-8. Setting of Error Conditions, CC = 01 (Selector Channel)

Conditions	IOSTIW Stored	IOSTIW Status Field	ISS
Error on CAW, CCW Read	Yes	Channel: Invalid Address or Channel Control Check or Program Check.	Attempted
Channel detected error on I/O interface	Yes	Channel: Interface Control Check	Attempted
Control Unit develops error status during ISS	Yes	Device: Status not equal to "Available Subsystem" status or Status ≠ xxxl xxxx (X bits, 0 or 1)	Yes

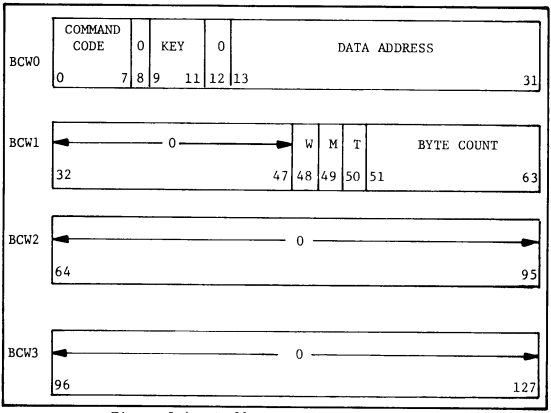

Figure 5-4. Buffer Control Word Format (Multiplexer Channel)

Table 5-9. Buffer Control Word Bit Assignments (Multiplexer Channel)

Field/Bit Ref. Fig.5-4	Description
Bits Ø-7 (Command Code)	The Command Code specifies the operation to be performed by the device and channel. The Command Code is transferred to the device during the Initial Selection Sequence of an SIO instruction. The Command Codes and their general interpretation are listed below. The M-bits are not interpreted by the channel.
Bit 8	Unassigned, must be set to zero.
Bits 9-11 (Key)	I/O Storage Protection Key.
Bit 12	Unassigned, must be set to zero.
Bits 13-31 (Data Address)	Field allows multiplexer channel to reference any byte in main storage during data transfer sequences. The address is updated by the channel during each data transfer sequence.
Bits 32-47	Unassigned, must be set to zero.
Bits 48 (W)	W = 0 Input Operation (Read) W = 1 Output Operation (Write) Channel sets bit on basis of Command Code byte. Program must initialize this bit to zero.
Bit 49 (M)	M = 0 Ascending Address (forward sequence) M = 1 Descending Address (reverse sequence)

Command Code Bits 0123	Command Code Bits 4567	Command
MMMM	0100	Sense
MMM	MM01	Write
MMMM	MM10	Read
MMMM	1100	Read Backward
MMMM	MM11	Control
MMMM	0000	Test
MMMM	1000	Transfer in Channel (TIC)

Table 5-9. Buffer Control Word Bit Assignments (Multiplexer Channel) (cont)

Field/Bit Ref.Fig.5-4	Description
Bit 50 (T)	T = Ø Transfer Data T = 1 Termination of Data Transfer Normal data transfer operations require the T bit to be set to zero by the software. The channel will be set to zero by the software. The channel will set T = 1 only when the transfer to a byte of data causes the Byte Count to go to zero. The channel will not set T = 0. If no data transfer is to take place, the T bit can be initialized to one by the software.
Bits 51-63 (Byte Count)	A thirteen bit field which contains the byte count which is required for all data transfer operations. The channel decrements the count during each data transfer sequence. An initial count of zero provides for a maximum transfer of 8192 bytes (if the I bit equals zero). When the channel decrements the byte count to zero it sets the T bit equal to one.
Bits 64-127	Unassigned, must be set to zero.

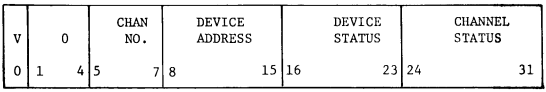

Figure 5-5. IOSTIW Format (Multiplexer Channel)

Table 5-10. Multiplexer Channel IOSTIW Description

<table>
<tr><th>Bit</th><th>Field</th><th>Description</th></tr>
<tr><td>0</td><td>V</td><td>Validation bit. Set to zero by the multiplexer channel before the IOSTIW is stored.</td></tr>
<tr><td>1 - 4</td><td></td><td>Unassigned, must be zeros.</td></tr>
<tr><td>5 - 7</td><td>Channel Number</td><td>Multiplexer channel number = 001</td></tr>
<tr><td>8 - 15</td><td>Device Address</td><td>Contains the device and subchannel addresses associated with the status information.</td></tr>
<tr><td>16 - 23</td><td>Device Status</td><td>
<table>
<tr><td>0</td><td>16</td><td>Attention</td></tr>
<tr><td>1</td><td>17</td><td>Status Modifier</td></tr>
<tr><td>2</td><td>18</td><td>Control Unit End</td></tr>
<tr><td>3</td><td>19</td><td>Busy</td></tr>
<tr><td>4</td><td>20</td><td>Channel End</td></tr>
<tr><td>5</td><td>21</td><td>Device End</td></tr>
<tr><td>6</td><td>22</td><td>Unit Check</td></tr>
<tr><td>7</td><td>23</td><td>Unit Exception</td></tr>
</table>
</td></tr>
<tr><td>24 - 31</td><td>Channel Status</td><td>
<table>
<tr><td>0</td><td>24</td><td>0</td></tr>
<tr><td>1</td><td>25</td><td>0</td></tr>
<tr><td>2</td><td>26</td><td>0</td></tr>
<tr><td>3</td><td>27</td><td>Invalid Address</td></tr>
<tr><td>4</td><td>28</td><td>Channel Data Check</td></tr>
<tr><td>5</td><td>29</td><td>Interface Control Check</td></tr>
<tr><td>6</td><td>30</td><td>Channel Control Check</td></tr>
<tr><td>7</td><td>31</td><td>0</td></tr>
</table>
</td></tr>
</table>

Table 5-11. SIO Condition Code (Multiplexer Channel)

CC	State*			Command Action	IOSTIW Stored	IOSTIW	Initial Selection Sequence
	Channel	Subchannel	Subsystem				
00	A	A	A	Accept	Yes	Device	Yes
01	A	A	P	Reject	Yes	Device	Yes
10	P	X	X	Reject	Yes	Channel	No
	A	A	W	Reject	No	-	Attempted (Immediate Busy)
11	N	X	X	Reject	No	-	No
	X	X	N	Reject	No	-	Attempted

*NOTE: A = Available
W = Working
P = Status Pending
N = Non-Operational
X = Any State

Table 5-12. SIO Reject Conditions (Multiplexer Channel)

Conditions	01_2 Condition Code Set; IOSTIW Stored	IOSTIW Status Field	ISS
Error on BCW Read	Yes	Channel: Invalid Address or Channel Control Check	No
Error on BCW Write	Yes	Channel: Invalid Address or Channel Control Check	Yes (1)
Channel detected error on I/O interface	Yes	Channel: Interface Control Check	Attempted (1)
Control unit develops error status during ISS	Yes (3)	Device: Status ≠ 0000 XX00 or Status ≠ XXX1 XXXX (X bits, 0 or 1)	Yes (2)

NOTES:

(1) Multiplexer channel issues Selective Reset.

(2) If device status is not pending in the channel, status is accepted. If device status is pending in the channel, status is stacked at the control unit. Status is accepted later via a control unit initiated request.

(3) Error condition 4 may occur, during the same ISS, prior to error condition 3. Both channel status and device status would be presented to the IOST in separate IOSTIW's - channel status first.

SECTION 6

FOLDOUT ILLUSTRATIONS

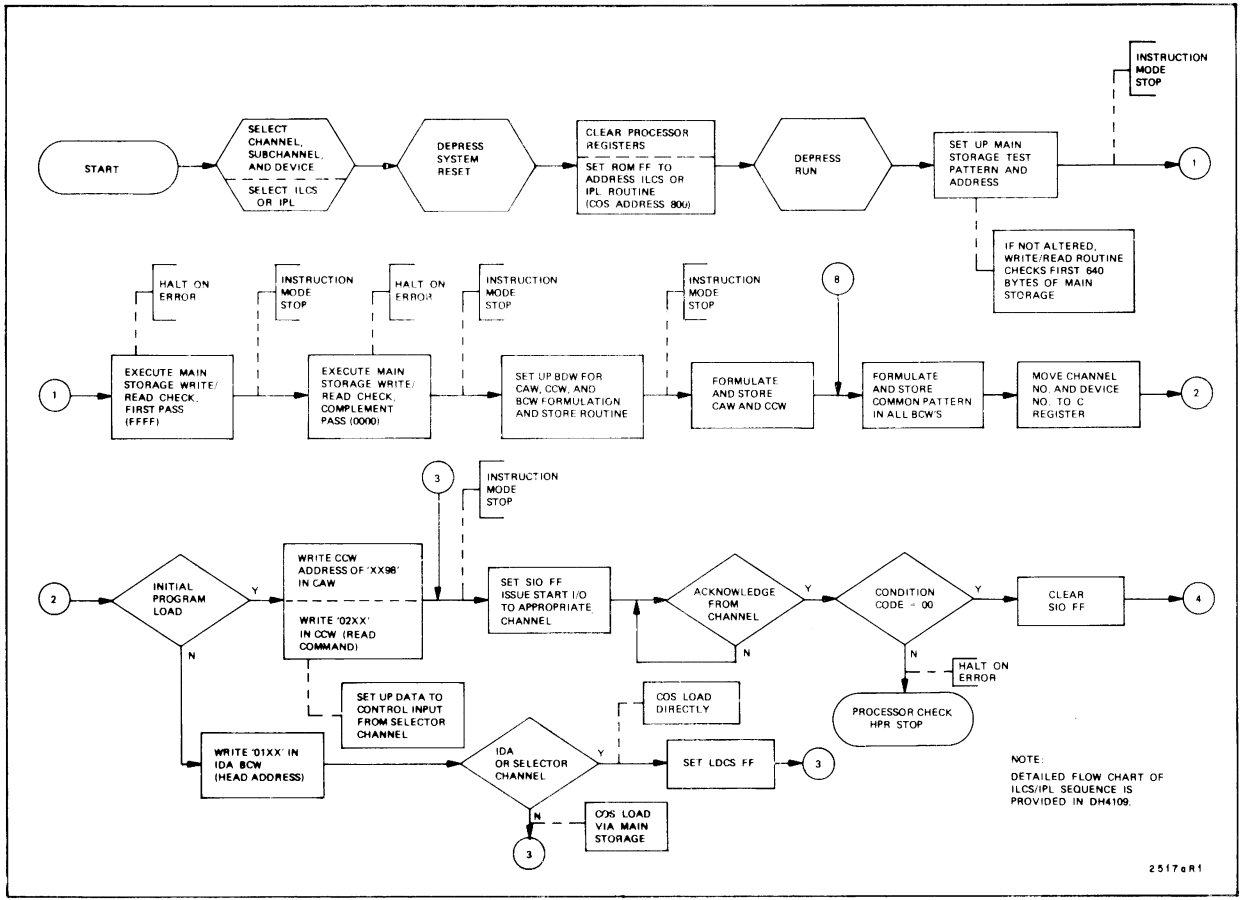
START
SELECT CHANNEL, SUBCHANNEL, AND DEVICE
SELECT ILCS OR IPL
DEPRESS SYSTEM RESET
CLEAR PROCESSOR REGISTERS
SET ROM FF TO ADDRESS ILCS OR IPL ROUTINE (COS ADDRESS 800)
DEPRESS RUN
SET UP MAIN STORAGE TEST PATTERN AND ADDRESS
INSTRUCTION MODE STOP
IF NOT ALTERED, WRITE/READ ROUTINE CHECKS FIRST 640 BYTES OF MAIN STORAGE
HALT ON ERROR
INSTRUCTION MODE STOP
HALT ON ERROR
INSTRUCTION MODE STOP
INSTRUCTION MODE STOP
EXECUTE MAIN STORAGE WRITE/READ CHECK, FIRST PASS (FFFF)
EXECUTE MAIN STORAGE WRITE/READ CHECK, COMPLEMENT PASS (0000)
SET UP BCW FOR CAW, CCW, AND BCW FORMULATION AND STORE ROUTINE
FORMULATE AND STORE CAW AND CCW
FORMULATE AND STORE COMMON PATTERN IN ALL BCW'S
MOVE CHANNEL NO. AND DEVICE NO. TO C REGISTER
INSTRUCTION MODE STOP
INITIAL PROGRAM LOAD
Y
N
WRITE CCW ADDRESS OF 'XX98' IN CAW
WRITE '02XX' IN CCW (READ COMMAND)
SET SIO FF ISSUE START I/O TO APPROPRIATE CHANNEL
ACKNOWLEDGE FROM CHANNEL
CONDITION CODE = 00
CLEAR SIO FF
HALT ON ERROR
PROCESSOR CHECK HPR STOP
SET UP DATA TO CONTROL INPUT FROM SELECTOR CHANNEL
WRITE '01XX' IN IDA BCW (HEAD ADDRESS)
IDA OR SELECTOR CHANNEL
COS LOAD DIRECTLY
SET LDCS FF
COS LOAD VIA MAIN STORAGE
NOTE:
DETAILED FLOW CHART OF ILCS/IPL SEQUENCE IS PROVIDED IN DH4109.
2517aR1

Figure 1-7
Initial Load of Control Storage/Initial Program Load
General Operational Sequence (3029-00,-01,-02,-03 90/30)
(Sheet 1 of 2)

MH2438

REVISION: HCB-2

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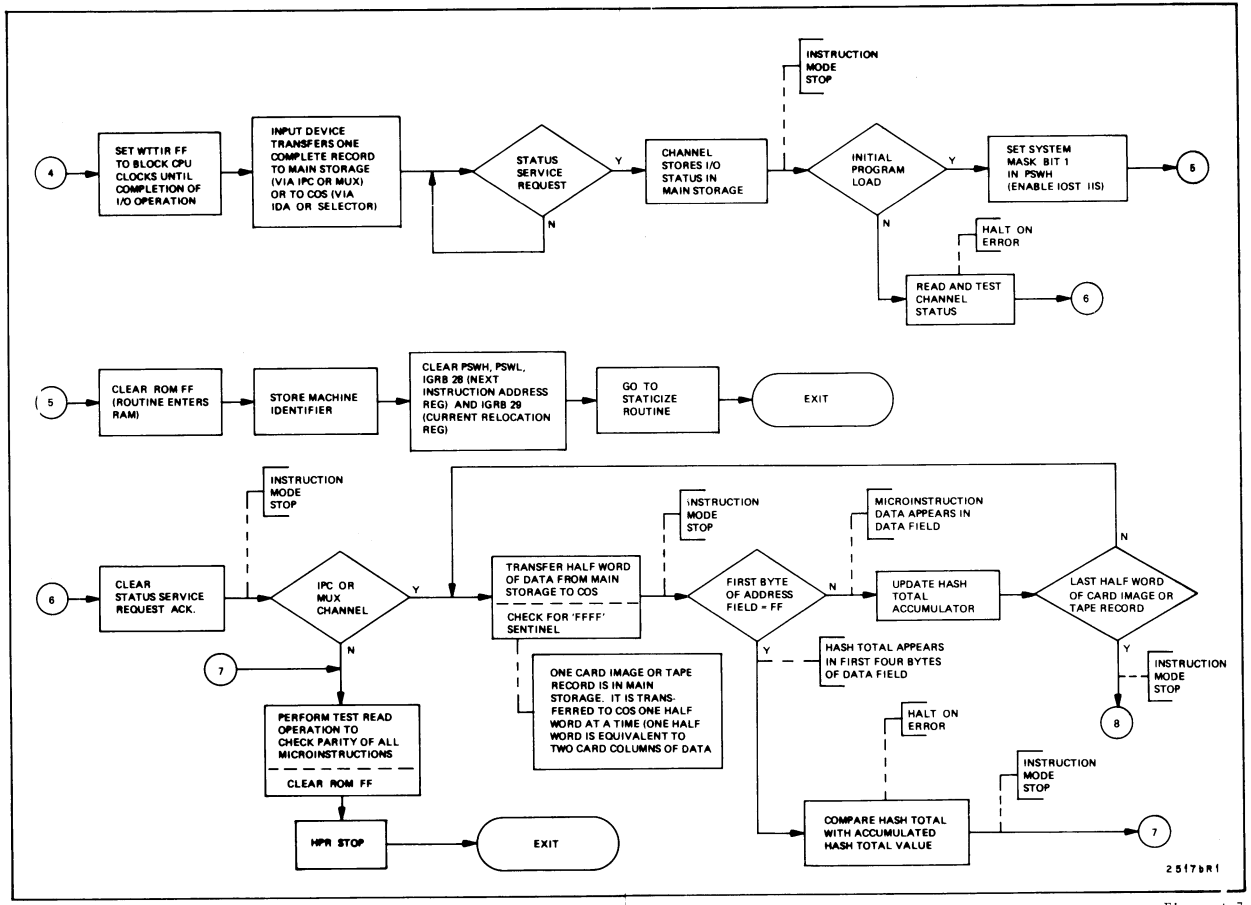
4
SET WTTIR FF TO BLOCK CPU CLOCKS UNTIL COMPLETION OF I/O OPERATION
INPUT DEVICE TRANSFERS ONE COMPLETE RECORD TO MAIN STORAGE (VIA IPC OR MUX) OR TO COS (VIA IDA OR SELECTOR)
STATUS SERVICE REQUEST
Y
N
CHANNEL STORES I/O STATUS IN MAIN STORAGE
INSTRUCTION MODE STOP
INITIAL PROGRAM LOAD
Y
N
SET SYSTEM MASK BIT 1 IN PSWH (ENABLE IOST IIS)
5
HALT ON ERROR
READ AND TEST CHANNEL STATUS
6
5
CLEAR ROM FF (ROUTINE ENTERS RAM)
STORE MACHINE IDENTIFIER
CLEAR PSWH, PSWL, IGRB 28 (NEXT INSTRUCTION ADDRESS REG) AND IGRB 29 (CURRENT RELOCATION REG)
GO TO STATICIZE ROUTINE
EXIT
6
CLEAR STATUS SERVICE REQUEST ACK.
INSTRUCTION MODE STOP
IPC OR MUX CHANNEL
Y
N
7
PERFORM TEST READ OPERATION TO CHECK PARITY OF ALL MICROINSTRUCTIONS
CLEAR ROM FF
HPR STOP
EXIT
TRANSFER HALF WORD OF DATA FROM MAIN STORAGE TO COS
CHECK FOR 'FFFF' SENTINEL
ONE CARD IMAGE OR TAPE RECORD IS IN MAIN STORAGE. IT IS TRANSFERRED TO COS ONE HALF WORD AT A TIME (ONE HALF WORD IS EQUIVALENT TO TWO CARD COLUMNS OF DATA
INSTRUCTION MODE STOP
FIRST BYTE OF ADDRESS FIELD = FF
Y
N
HASH TOTAL APPEARS IN FIRST FOUR BYTES OF DATA FIELD
MICROINSTRUCTION DATA APPEARS IN DATA FIELD
UPDATE HASH TOTAL ACCUMULATOR
LAST HALF WORD OF CARD IMAGE OR TAPE RECORD
N
Y
INSTRUCTION MODE STOP
8
HALT ON ERROR
INSTRUCTION MODE STOP
COMPARE HASH TOTAL WITH ACCUMULATED HASH TOTAL VALUE
7
2517bR1

Figure 1-7
Initial Load of Control Storage/Initial Program Load
General Operational Sequence (3029-00,-01,-02,-03 90/30)
(Sheet 2 of 2)

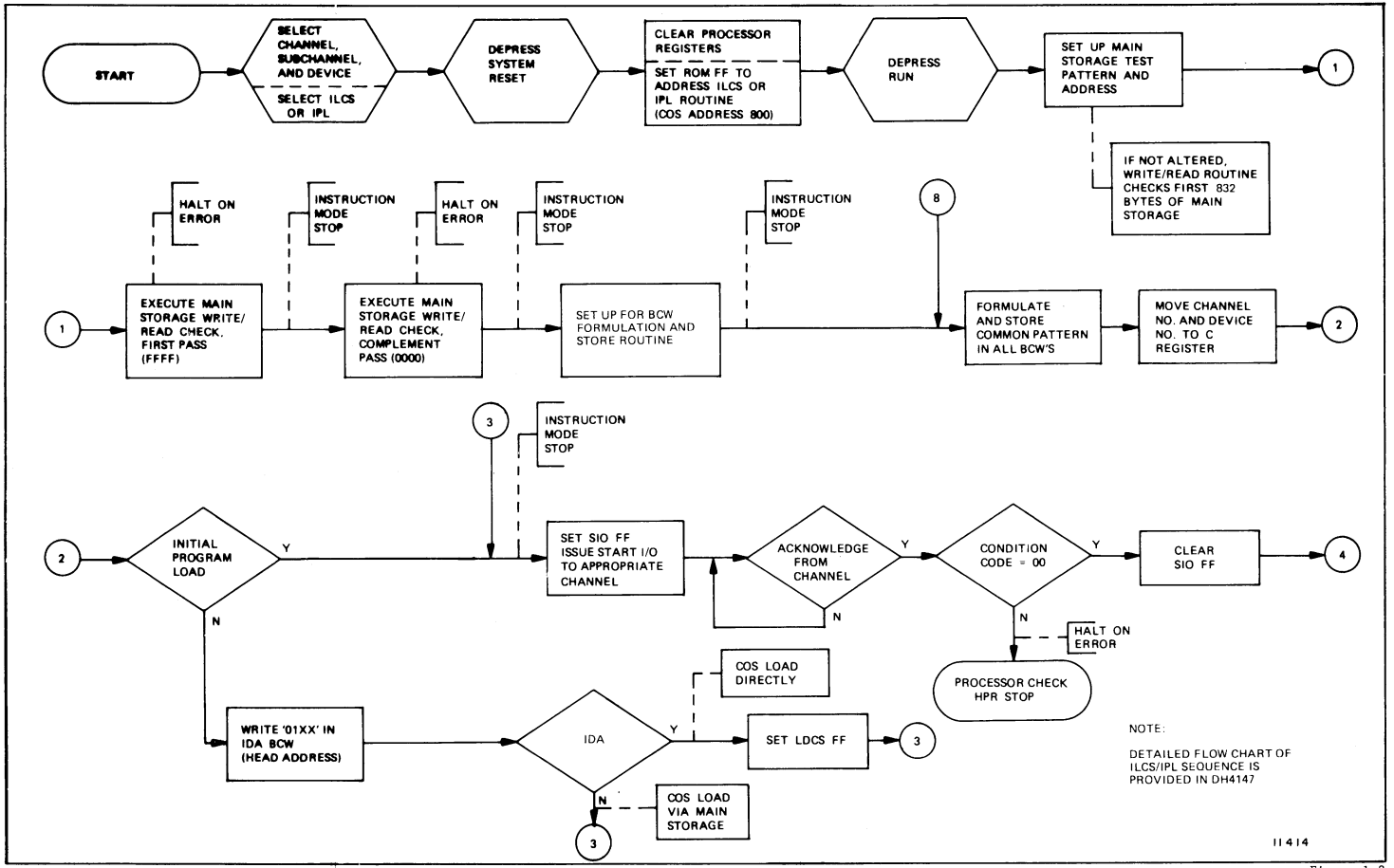

Figure 1-8
Initial Load of Control Storage/Initial Program Load
General Operational Sequence (3029-02,-03 90/25 and 90/30B)
(Sheet 1 of 2)

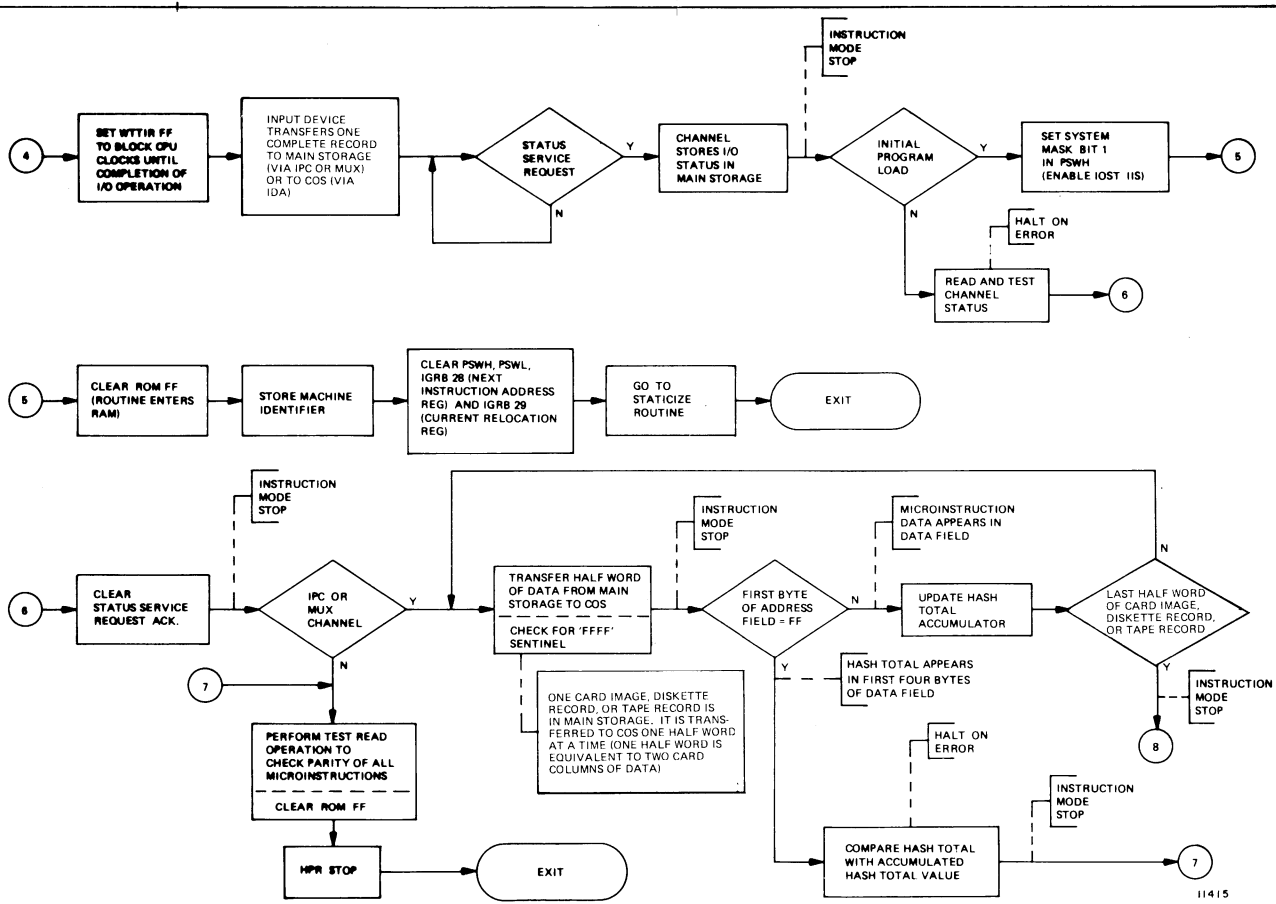
4
SET WTTIR FF TO BLOCK CPU CLOCKS UNTIL COMPLETION OF I/O OPERATION
INPUT DEVICE TRANSFERS ONE COMPLETE RECORD TO MAIN STORAGE (VIA IPC OR MUX) OR TO COS (VIA IDA)
STATUS SERVICE REQUEST
Y
N
CHANNEL STORES I/O STATUS IN MAIN STORAGE
INSTRUCTION MODE STOP
INITIAL PROGRAM LOAD
Y
N
SET SYSTEM MASK BIT 1 IN PSWH (ENABLE IOST IIS)
5
HALT ON ERROR
READ AND TEST CHANNEL STATUS
6
5
CLEAR ROM FF (ROUTINE ENTERS RAM)
STORE MACHINE IDENTIFIER
CLEAR PSWH, PSWL, IGRB 28 (NEXT INSTRUCTION ADDRESS REG) AND IGRB 29 (CURRENT RELOCATION REG)
GO TO STATICIZE ROUTINE
EXIT
6
CLEAR STATUS SERVICE REQUEST ACK.
INSTRUCTION MODE STOP
IPC OR MUX CHANNEL
Y
N
7
PERFORM TEST READ OPERATION TO CHECK PARITY OF ALL MICROINSTRUCTIONS
CLEAR ROM FF
HPR STOP
EXIT
TRANSFER HALF WORD OF DATA FROM MAIN STORAGE TO COS
CHECK FOR 'FFFF' SENTINEL
ONE CARD IMAGE, DISKETTE RECORD, OR TAPE RECORD IS IN MAIN STORAGE. IT IS TRANSFERRED TO COS ONE HALF WORD AT A TIME (ONE HALF WORD IS EQUIVALENT TO TWO CARD COLUMNS OF DATA)
INSTRUCTION MODE STOP
FIRST BYTE OF ADDRESS FIELD = FF
Y
N
HASH TOTAL APPEARS IN FIRST FOUR BYTES OF DATA FIELD
MICROINSTRUCTION DATA APPEARS IN DATA FIELD
UPDATE HASH TOTAL ACCUMULATOR
LAST HALF WORD OF CARD IMAGE, DISKETTE RECORD, OR TAPE RECORD
N
Y
INSTRUCTION MODE STOP
8
HALT ON ERROR
INSTRUCTION MODE STOP
COMPARE HASH TOTAL WITH ACCUMULATED HASH TOTAL VALUE
7
11415

Figure 1-8
Initial Load of Control Storage/Initial Program Load
General Operational Sequence (3029-02,-03 90/25 and 90/30B)
(Sheet 2 of 2)

MH2438

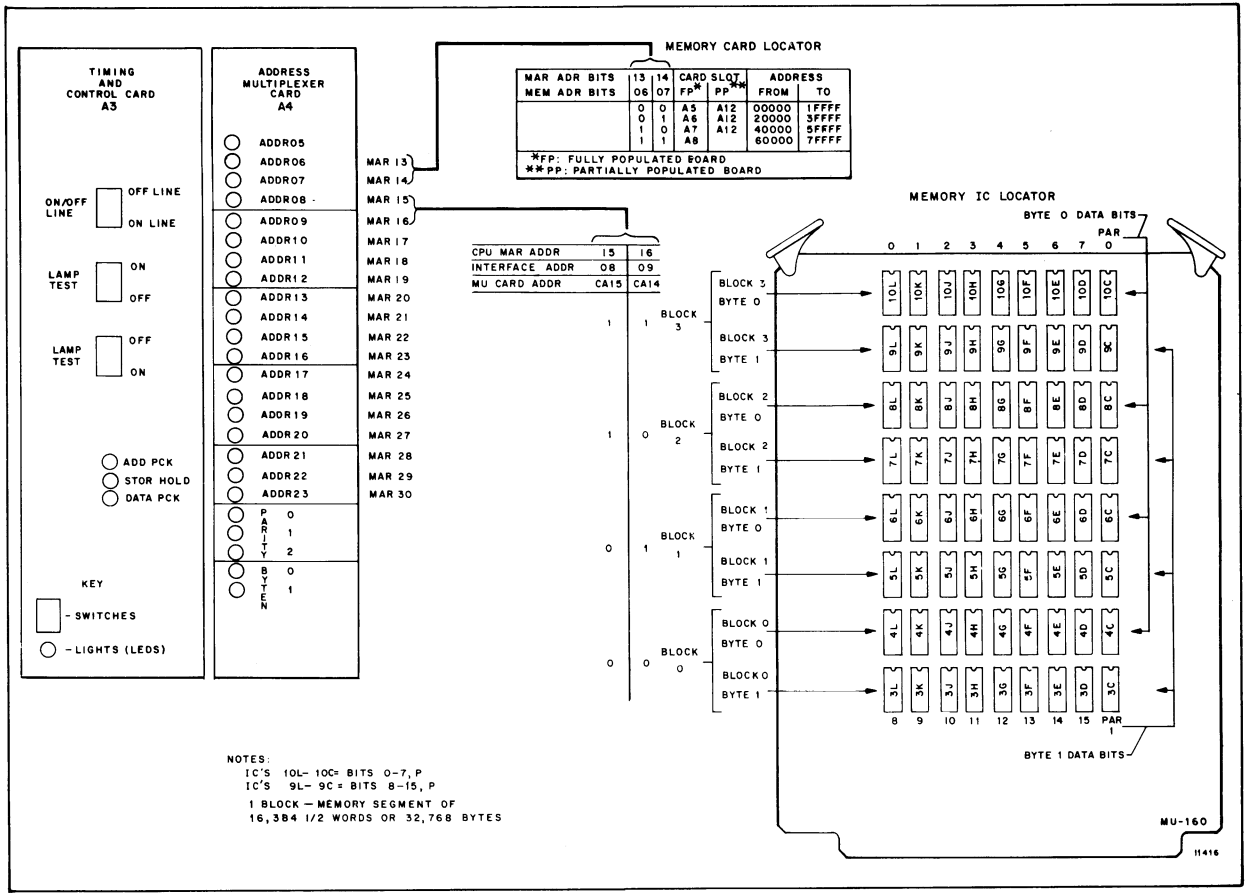

Figure 2-9
MU160 Main Storage Addressing Scheme
(3029-02,-03 90/25, 90/30, and 90/30B)
REVISION: HCB-2

MH2438

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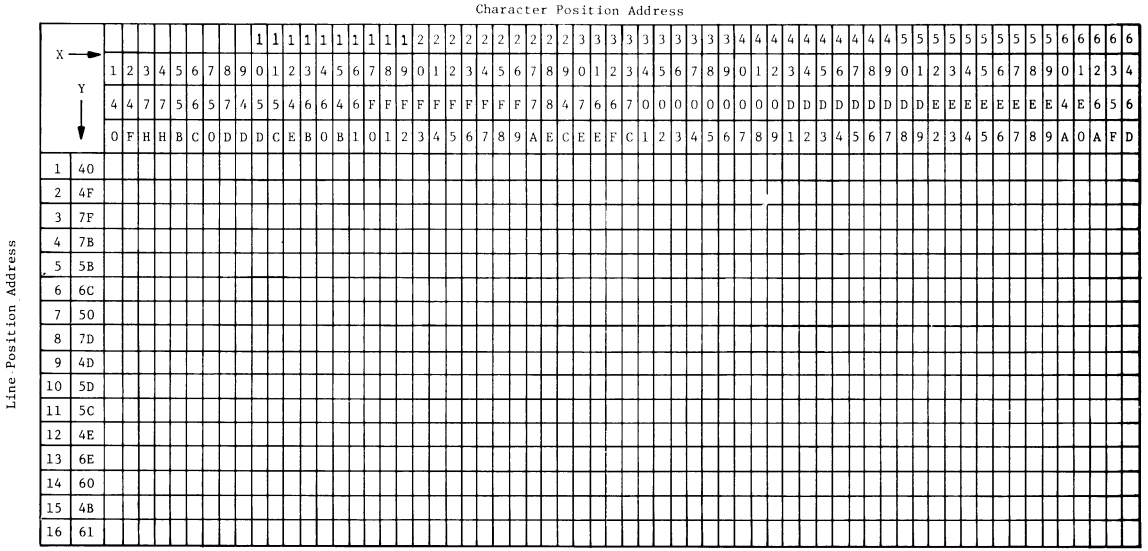

NOTE: To position the Cursor using the processor, the following character sequence must be transmitted.

Character	ESC	VT	X	Y	S
Hex Code	27	0B	XX_{16}	YY_{16}	0F

XX and YY values designate the Cursor position.

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Figure 3-8
U100 Console Cursor Addressing For Screen Display
REVISION: HCB-2

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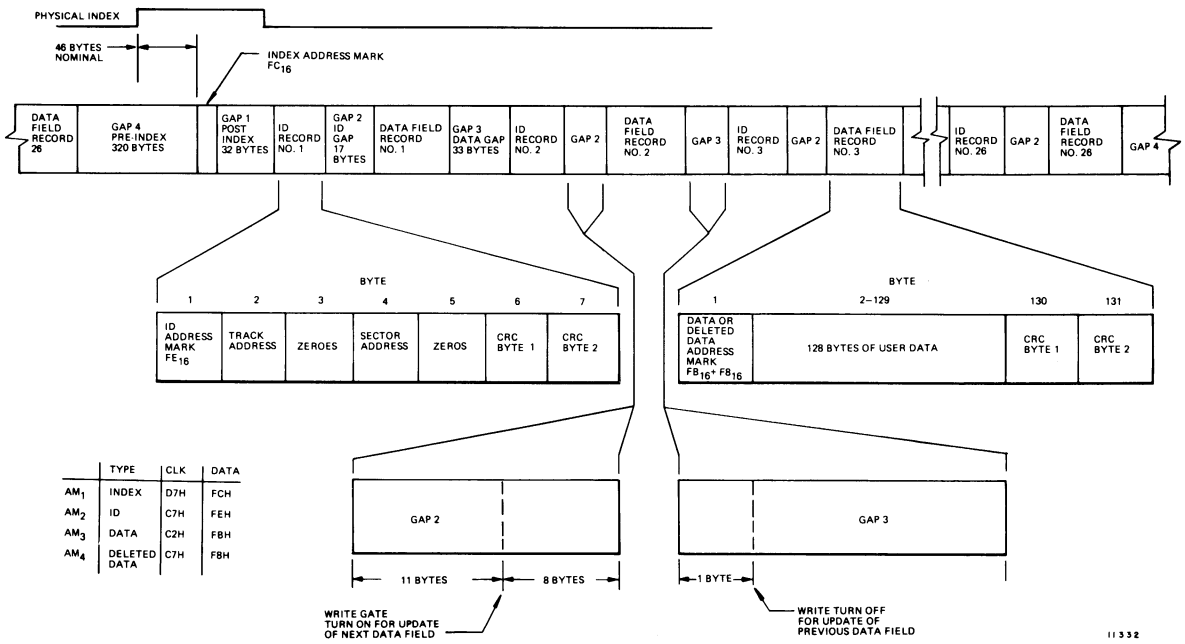

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Figure 3-14
8413 Diskette FM Track Format

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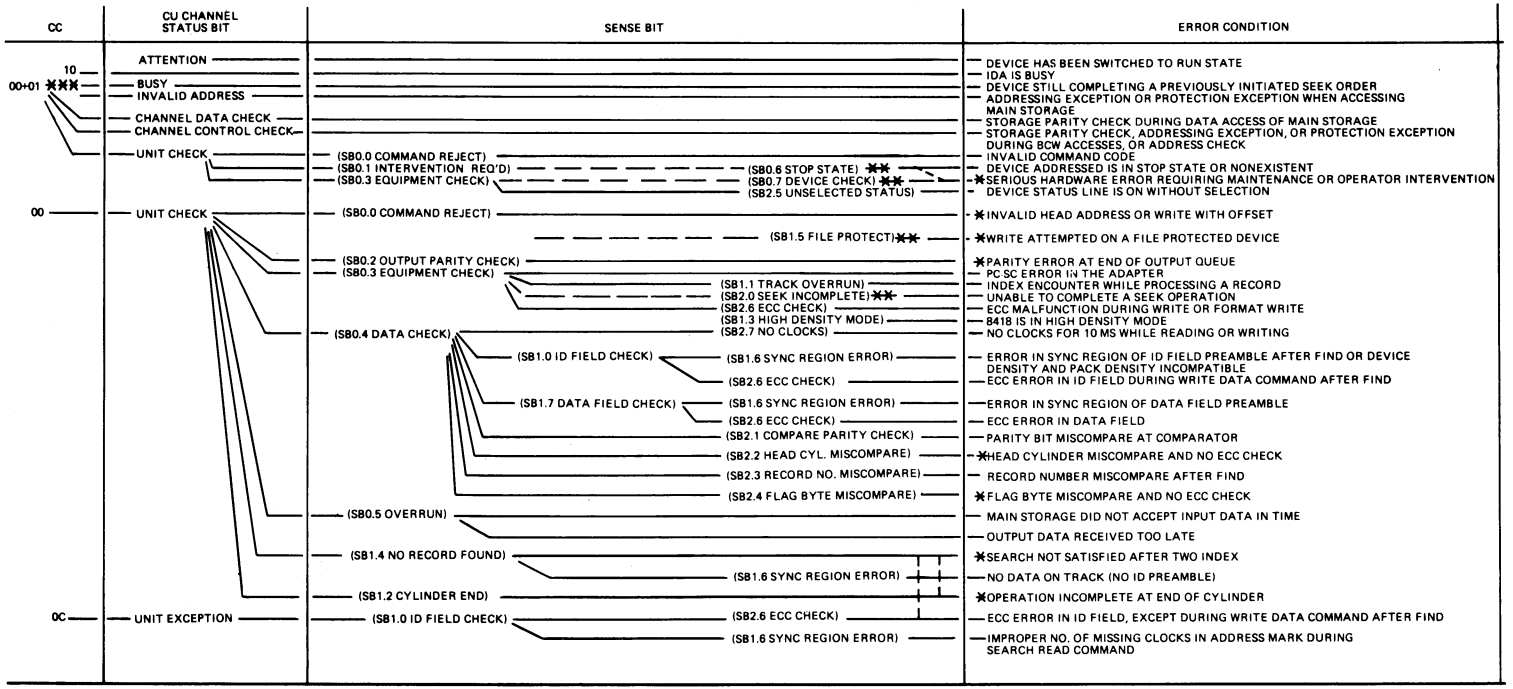
CC
CU CHANNEL STATUS BIT
SENSE BIT
ERROR CONDITION
10
ATTENTION
DEVICE HAS BEEN SWITCHED TO RUN STATE
00+01 ✱✱✱
BUSY
IDA IS BUSY
INVALID ADDRESS
DEVICE STILL COMPLETING A PREVIOUSLY INITIATED SEEK ORDER
ADDRESSING EXCEPTION OR PROTECTION EXCEPTION WHEN ACCESSING MAIN STORAGE
CHANNEL DATA CHECK
STORAGE PARITY CHECK DURING DATA ACCESS OF MAIN STORAGE
CHANNEL CONTROL CHECK
STORAGE PARITY CHECK, ADDRESSING EXCEPTION, OR PROTECTION EXCEPTION DURING BCW ACCESSES, OR ADDRESS CHECK
UNIT CHECK
(SB0.0 COMMAND REJECT)
INVALID COMMAND CODE
(SB0.1 INTERVENTION REQ'D)
(SB0.6 STOP STATE) ✱✱
DEVICE ADDRESSED IS IN STOP STATE OR NONEXISTENT
(SB0.3 EQUIPMENT CHECK)
(SB0.7 DEVICE CHECK) ✱✱
✱SERIOUS HARDWARE ERROR REQUIRING MAINTENANCE OR OPERATOR INTERVENTION
(SB2.5 UNSELECTED STATUS)
DEVICE STATUS LINE IS ON WITHOUT SELECTION
00
UNIT CHECK
(SB0.0 COMMAND REJECT)
✱INVALID HEAD ADDRESS OR WRITE WITH OFFSET
(SB1.5 FILE PROTECT) ✱✱
✱WRITE ATTEMPTED ON A FILE PROTECTED DEVICE
(SB0.2 OUTPUT PARITY CHECK)
✱PARITY ERROR AT END OF OUTPUT QUEUE
(SB0.3 EQUIPMENT CHECK)
PCSC ERROR IN THE ADAPTER
(SB1.1 TRACK OVERRUN)
INDEX ENCOUNTER WHILE PROCESSING A RECORD
(SB2.0 SEEK INCOMPLETE) ✱✱
UNABLE TO COMPLETE A SEEK OPERATION
(SB2.6 ECC CHECK)
ECC MALFUNCTION DURING WRITE OR FORMAT WRITE
(SB1.3 HIGH DENSITY MODE)
8418 IS IN HIGH DENSITY MODE
(SB0.4 DATA CHECK)
(SB2.7 NO CLOCKS)
NO CLOCKS FOR 10 MS WHILE READING OR WRITING
(SB1.0 ID FIELD CHECK)
(SB1.6 SYNC REGION ERROR)
ERROR IN SYNC REGION OF ID FIELD PREAMBLE AFTER FIND OR DEVICE DENSITY AND PACK DENSITY INCOMPATIBLE
(SB2.6 ECC CHECK)
ECC ERROR IN ID FIELD DURING WRITE DATA COMMAND AFTER FIND
(SB1.7 DATA FIELD CHECK)
(SB1.6 SYNC REGION ERROR)
ERROR IN SYNC REGION OF DATA FIELD PREAMBLE
(SB2.6 ECC CHECK)
ECC ERROR IN DATA FIELD
(SB2.1 COMPARE PARITY CHECK)
PARITY BIT MISCOMPARE AT COMPARATOR
(SB2.2 HEAD CYL. MISCOMPARE)
✱HEAD CYLINDER MISCOMPARE AND NO ECC CHECK
(SB2.3 RECORD NO. MISCOMPARE)
RECORD NUMBER MISCOMPARE AFTER FIND
(SB2.4 FLAG BYTE MISCOMPARE)
✱FLAG BYTE MISCOMPARE AND NO ECC CHECK
(SB0.5 OVERRUN)
MAIN STORAGE DID NOT ACCEPT INPUT DATA IN TIME
OUTPUT DATA RECEIVED TOO LATE
(SB1.4 NO RECORD FOUND)
✱SEARCH NOT SATISFIED AFTER TWO INDEX
(SB1.6 SYNC REGION ERROR)
NO DATA ON TRACK (NO ID PREAMBLE)
(SB1.2 CYLINDER END)
✱OPERATION INCOMPLETE AT END OF CYLINDER
0C
UNIT EXCEPTION
(SB1.0 ID FIELD CHECK)
(SB2.6 ECC CHECK)
ECC ERROR IN ID FIELD, EXCEPT DURING WRITE DATA COMMAND AFTER FIND
(SB1.6 SYNC REGION ERROR)
IMPROPER NO. OF MISSING CLOCKS IN ADDRESS MARK DURING SEARCH READ COMMAND

NOTES:

✱ERROR MAY BE CAUSED BY SOFTWARE.
✱✱REFLECTS CURRENT STATE OF THE DEVICE. SETS BIT ON LEFT ONLY WHEN INDICATING AN ERROR AS A RESULT OF A COMMAND.
– – – – CONNECTED SENSE BITS OR ERROR CONDITIONS MAY OCCUR TOGETHER OR SEPARATELY.
✱✱✱BUSY, COMMAND REJECT, OR INTERVENTION REQ'D WILL ALWAYS RESULT IN CC01.

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Figure 4-3
Summary of Status Bits, Sense Bits, and Error Conditions (IDA)